MITSUBISHI ELECTRIC

IPM L1/S1-series

APPLICATION NOTE

Sep. 2008

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1.Product Line-up

L1-series IPM

7pack (Inverter+ Brake)

600V (AC200)		1200V (AC400V)	
Screw type	Pin type	Screw type	Pin type
	PM50RL1C060		PM25RL1C120
PM50RL1A060	PM50RL1B060	PM25RL1A120	PM25RL1B120
PM75RL1A060	PM75RL1B060	PM50RL1A120	PM50RL1B120
PM100RL1A060	PM100RL1B060	PM75RL1A120	PM75RL1B120
PM150RL1A060	PM150RL1B060	PM100RL1A120	
PM200RL1A060		PM150RL1A120	
PM300RL1A060			

6pack (Inverter)

600V (AC200)		1200V (AC400V)	
Screw type	Pin type	Screw type	Pin type
PM50CL1A060	PM50CL1B060	PM25CL1A120	PM25CL1B120
PM75CL1A060	PM75CL1B060	PM50CL1A120	PM50CL1B120
PM100CL1A060	PM100CL1B060	PM75CL1A120	PM75CL1B120
PM150CL1A060	PM150CL1B060	PM100CL1A120	
PM200CL1A060		PM150CL1A120	
PM300CL1A060			

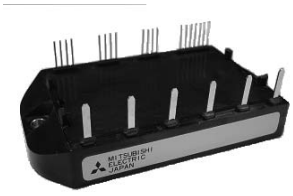
S1-series IPM

6pack (Inverter)

600V (AC200)	1200V (AC400V)
Screw type	Screw type
PM50CS1D060	PM25CS1D120
PM75CS1D060	PM50CS1D120
PM100CS1D060	PM75CS1D120
PM150CS1D060	PM100CS1D120
PM200CS1D060	

Package

IPM L1-series Mini-package



Small pin type package

IPM L1-series Small-package

Screw type package

Pin type package

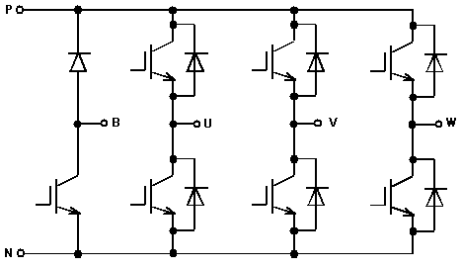
IPM L1-series Medium-package

Screw type package

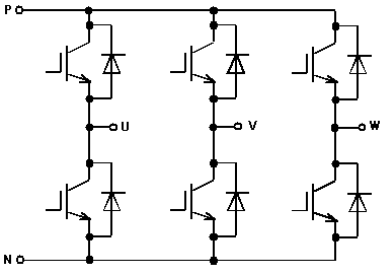
IPM S1-series package

Screw type package

2.Internal circuit



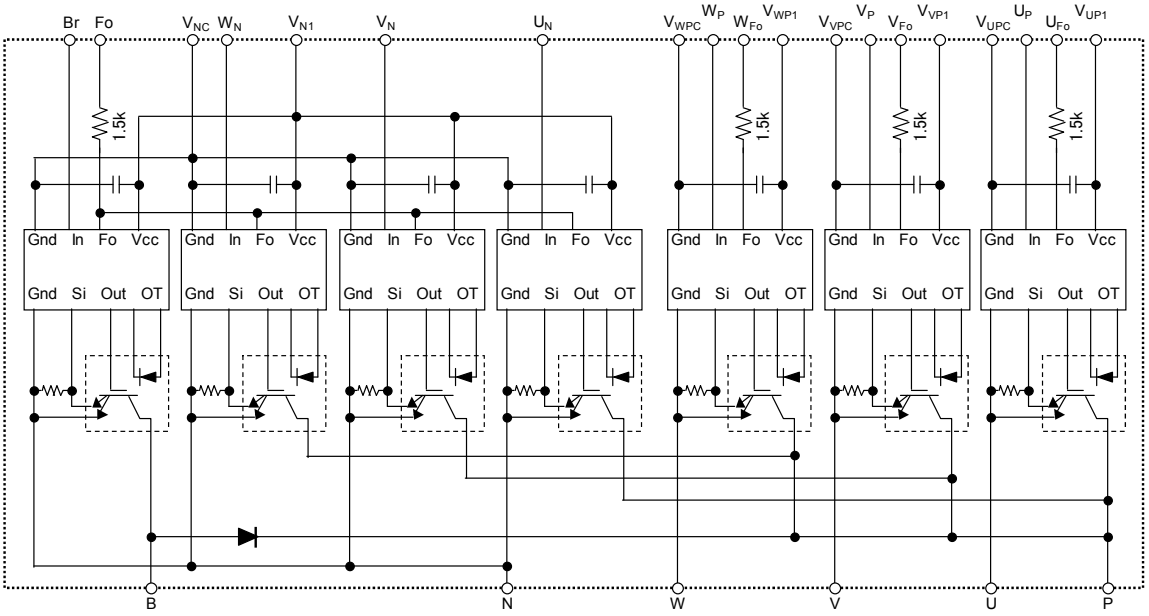
7pack (Inverter+ Brake)



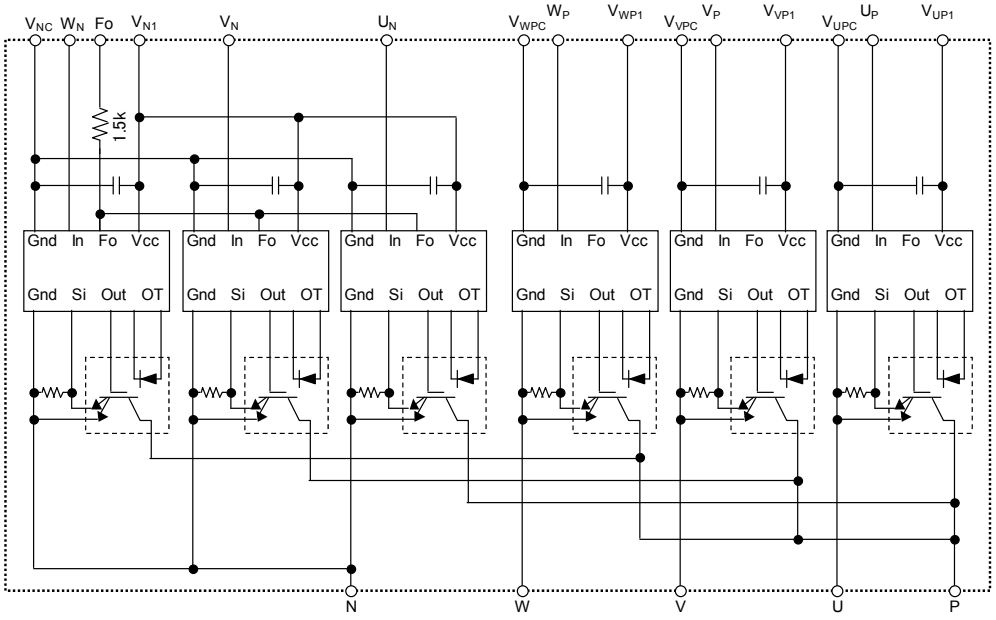
6pack (Inverter)

L1-series

Ex.) 7in1 type

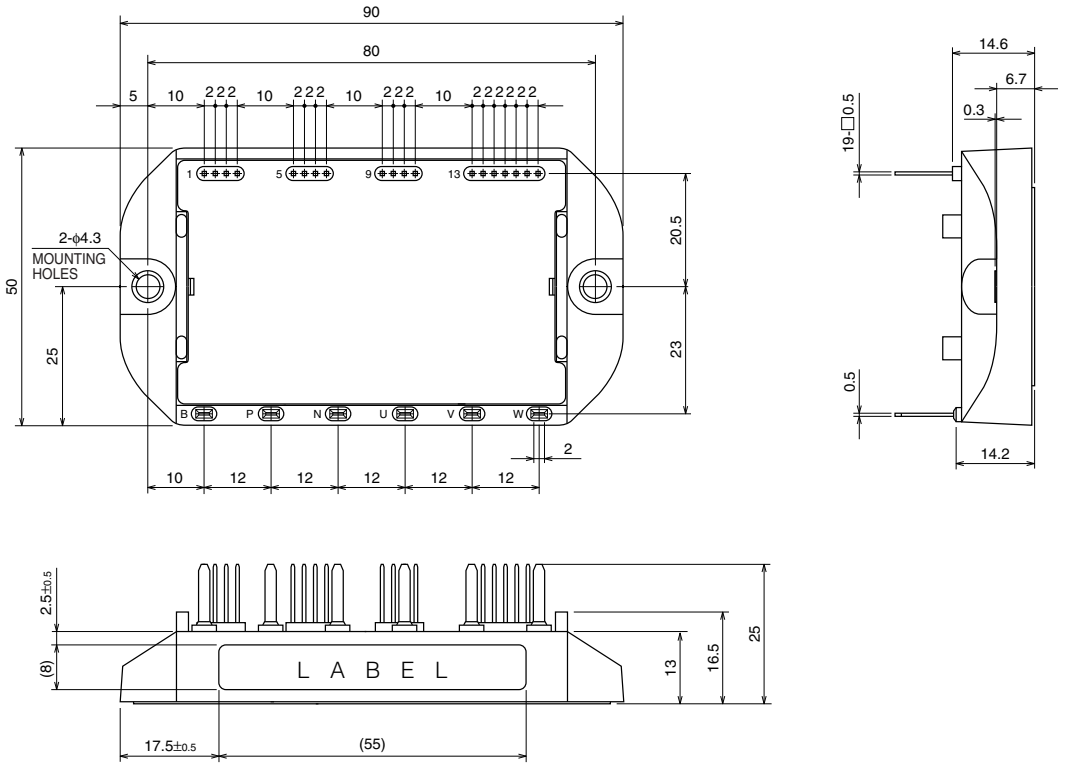


S1-series

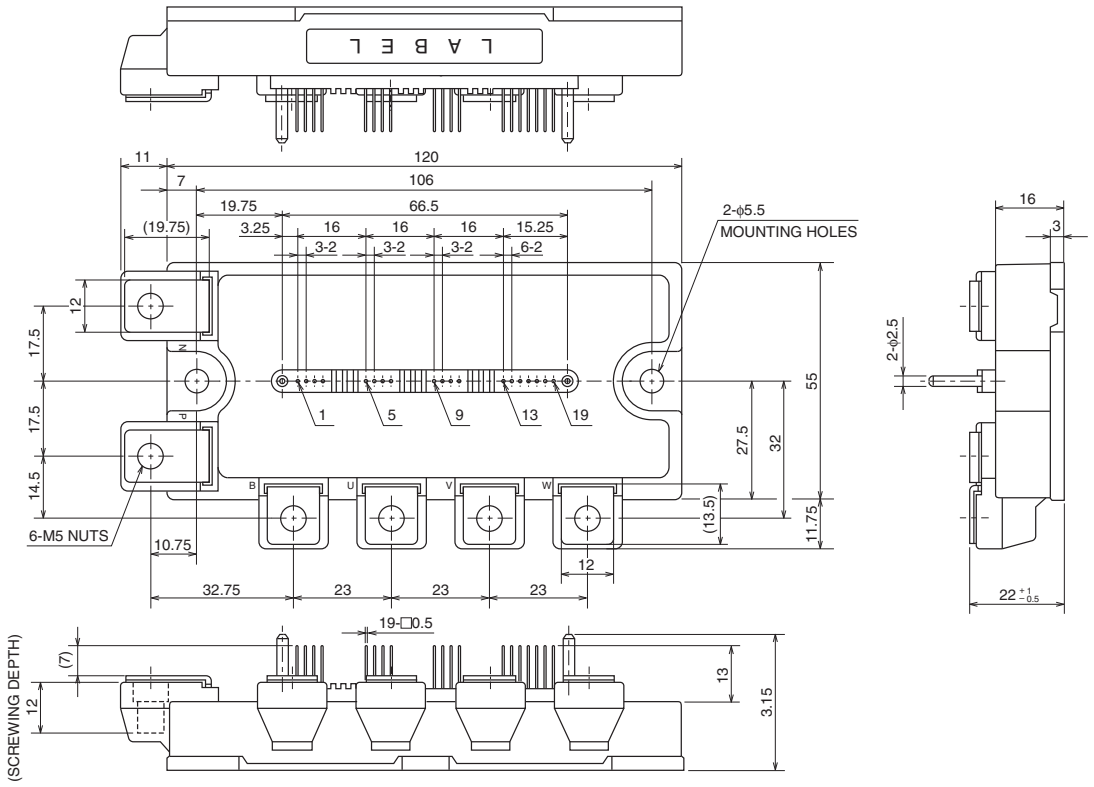


3.Package Outline

IPM L1-series Mini-package

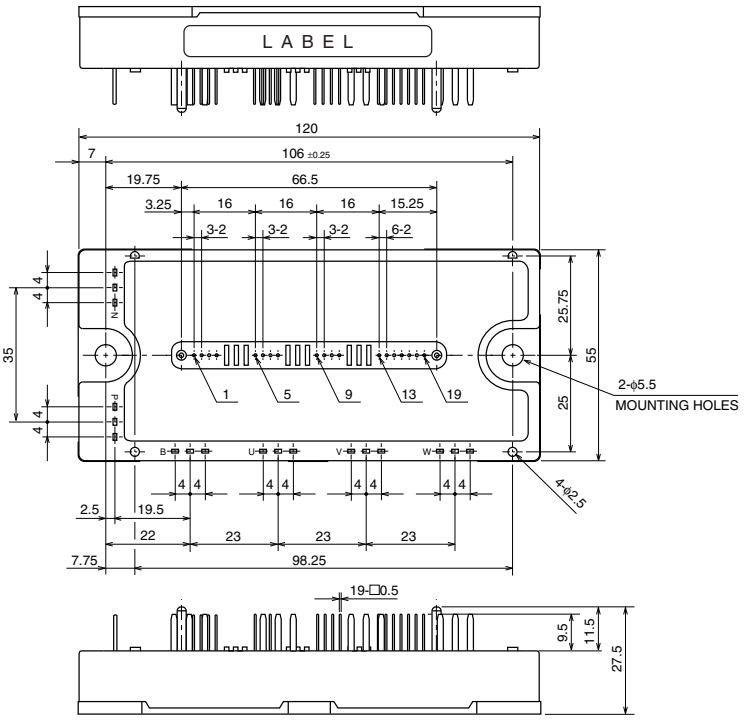


IPM L1-series Small-package (Screw type)

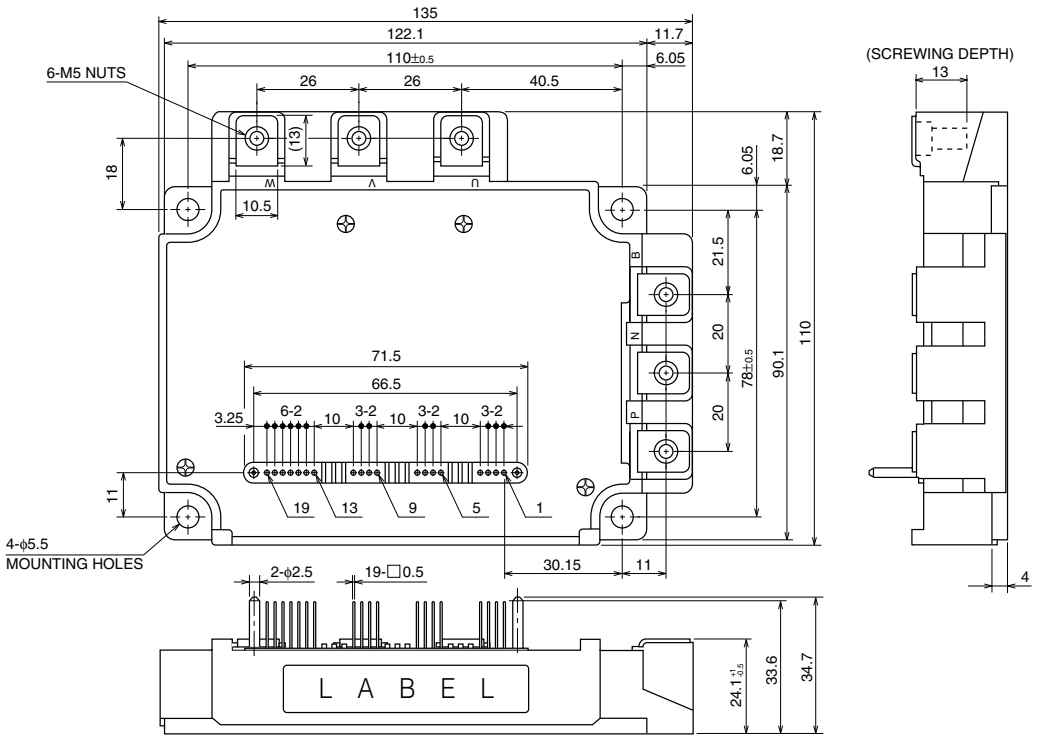


Package Outline

IPM L1-series Small-package (Pin type)

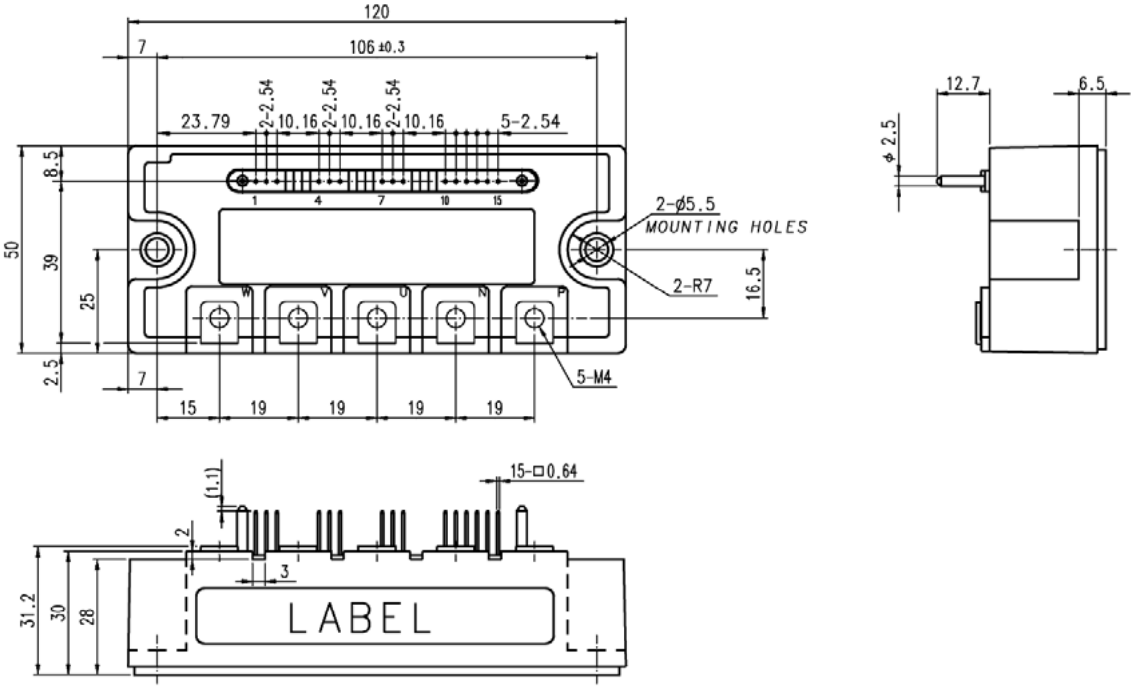


IPM L1-series Medium-package



Package Outline

IPM S1-series package



4.Applications of IPM to General purpose Inverter (reference)

■AC220V Line

Motor Ratings (kW)	For Inverter Module	For Converter Diode
	L1-series	
3.7	PM50RL1A060,PM50RL1B060 PM50CL1A060,PM50CL1B060 PM50RL1C060	RM30TA-H
5.5/7.5	PM75RL1A060,PM75RL1B060 PM75CL1A060,PM75CL1B060	RM30TA-H
11.0	PM100RL1A060,PM100RL1B060 PM100CL1A060,PM100CL1B060	RM50TC-H
15.0/18.5	PM150RL1A060,PM150RL1B060 PM150CL1A060,PM150CL1B060	RM75TC-H
22.0	PM200RL1A060,PM200CL1A060	RM75TC-H
30.0	PM300RL1A060,PM300CL1A060	PM100DZ-H × 3

■AC440V Line

Motor Ratings (kW)	For Inverter Module	For Converter Diode
	L1-series	
5.5	PM25RL1A120,PM25RL1B120 PM25CL1A120,PM25CL1B120 PM25RL1C120	RM20TA-2H
7.5	PM50RL1A120,PM50RL1B120 PM50CL1A120,PM50CL1B120	RM50TC-2H
11.0/15.0	PM75RL1A120,PM75RL1B120 PM75CL1A120,PM75CL1B120	RM50TC-2H
18.5/22.0	PM100RL1A120,PM100CL1A120	RM50TC-2H
30.0	PM150RL1A120,PM150CL1A120	PM60DZ-2H × 3

Applications of IPM to Servo Motor Controls (reference)

■AC220V Line

Motor Ratings (kW)	For Inverter Module	For Converter Diode
	S1-series	
~1.5	PM50CS1D060	RM30TA-H
~2.0	PM75CS1D060	RM30TA-H
~3.5	PM100CS1D060	RM50TC-H
~6.0	PM150CS1D060	RM75TC-H
~7.5	PM200CS1D060	RM75TC-H

■AC440V Line

Motor Ratings (kW)	For Inverter Module	For Converter Diode
	S1-series	
~1.5	PM25CS1D120	RM20TA-2H
~3.0	PM50CS1D120	RM50TC-2H
~5.0	PM75CS1D120	RM50TC-2H
~6.0	PM100CS1D120	RM50TC-2H

The above-mentioned tables are examples of the reference.
It is necessary to select the power-module (IPM) from the power-loss and the heat calculation result in the voltage, the current, and use conditions.

5. Term Explanation

General 1

Symbol		Definition
IGBT	Insulated Gate Bipolar Transistor	
FWDi	Free Wheeling Diode	anti-parallel to the IGBT
IPM	Intelligent Power Module	
tdead	Dead Time	Low side turn-off to high Side turn-on & High Side turn-off to low side turn-on
IPM Motor	Interior Permanent Magnet Motor	
CMR	Common Mode Noise Reduction	The maximum rise ratio of common mode voltage
CM_H		The maximum rise ratio of common mode voltage at the specific high level
CM_L		The maximum rise ratio of common mode voltage at the specific low level
CTR	Current Transfer Ratio	the ratio of the output current to the input current

General 2

Symbol	Parameter	Definition
T_a	Ambient Temperature	Atmosphere temperature without being subject to thermal source
T_c	Case Temperature	Case temperature measured at specified point

Absolute maximum Ratings

Symbol	Parameter	Definition
V_{CES}	Collector-Emitter Blocking Voltage	Maximum Off-state collector-emitter voltage at applied control input off signal
I_C	Continuous Collector Current	Maximum collector current – DC
I_{CP}	Peak Collector Current Repetitive	Peak collector current, Tj≤150°C
P_C	Power Dissipation	Maximum power dissipation, per device, T_C=25°C
T_j	Junction Temperature	Allowable range of IGBT junction temperature during operation
T_{stg}	Storage Temperature	Allowable range of temperature within which the module may be stored or transported without being subject to electrical load.
V_{iso}	Isolation Voltage	Minimum RMS isolation voltage capability applied electric terminal to base plate, 1 minute duration
-	Mounting Torque	Allowable tightening torque for terminal and mounting screws

※I_E and I_F are using by the difference of the connection and so on like the following figure.

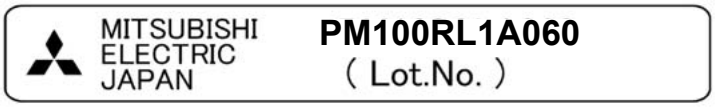
Electrical Characteristics

Symbol	Parameter	Definition
I_{CES}	Collector-Emitter Leakage Current	I_C at V_{CE} = V_{CES}, V_{CIN} = 15V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	V_{CE} at I_C = rated I_C and V_D = 15V
tc(on)	Turn-on Crossover Time	Time from I_C=10% to V_{CE}=10% of final value
tc(off)	Turn-off Crossover Time	Time from V_{CE}=10% to I_C=10% of final value
E_{on}	Turn-on Switching loss	Energy dissipated inside the IGBT during the turn-on of a single collector current pulse. Integral time starts from the 10% rise point of the collector current and ends at the 10% of the collector-emitter voltage point.
E_{off}	Turn-off Switching loss	Energy dissipated inside the IGBT during the turn-off of a single collector current pulse. Integral time starts from the 10% rise point of the collector-emitter voltage and ends at the 10% of the collector current point.
t_{rr}	Diode Reverse Recovery Time	Time from I_C=0A to projection of zero I_C from Irr and 0.5×Irr points with I_E = rated I_C.
V_{EC}	Forward Voltage Drop of Diode	V_{EC} at -I_C = rated Ic
R_{th}	Thermal Resistance	The rise of junction temperature per unit of power applied for a given time period
$R_{th(j-c)}$	Thermal Resistance, Junction to Case	I_C conducting to establish thermal equilibrium
$R_{th(c-f)}$	Thermal Resistance, Case to Fin	I_C conducting to establish thermal equilibrium lubricated

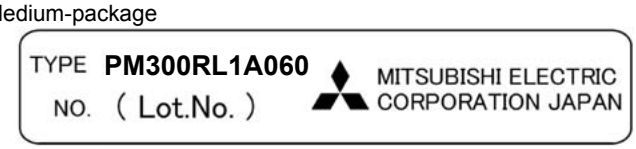
6. Numbering System

Label)

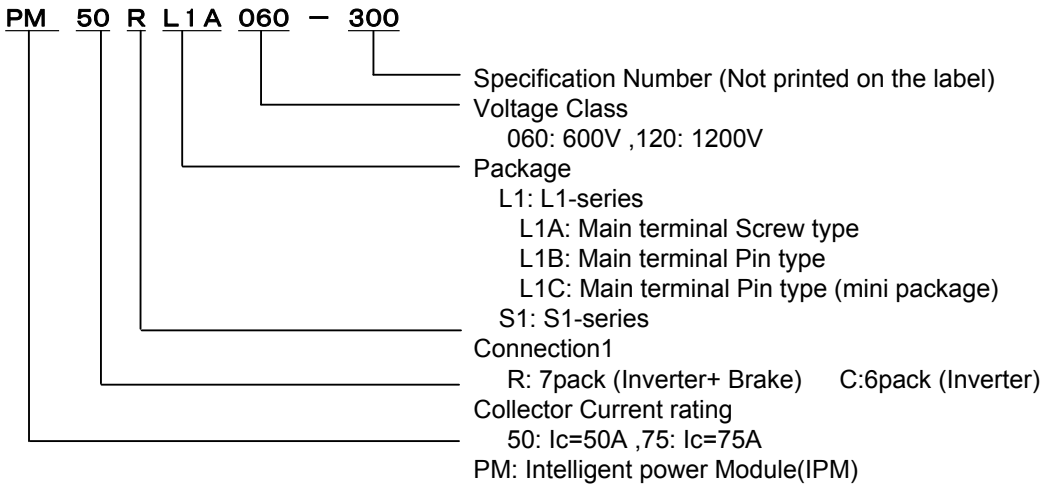
L1-series Mini-package ,L1-series Small-package, S1-series



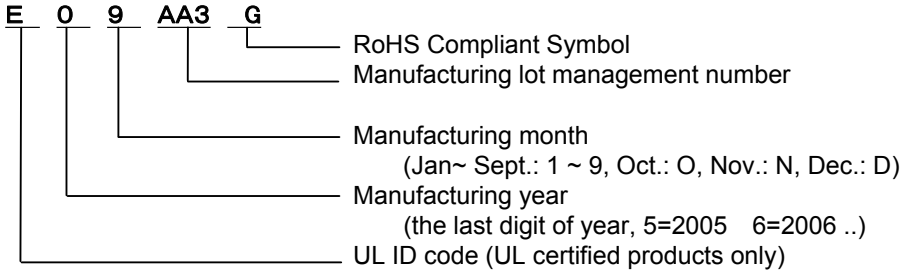
L1-series Medium-package



Type Name)

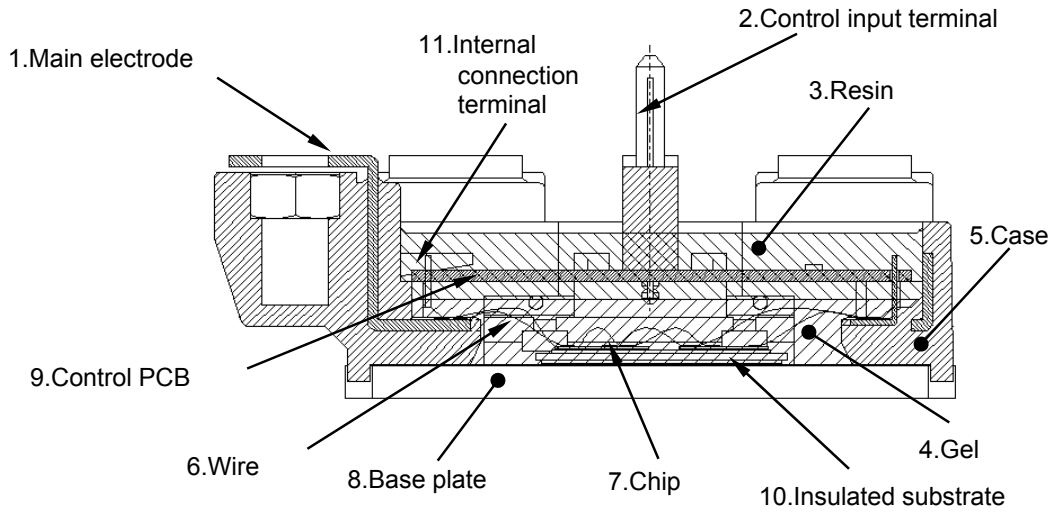


Lot Number)



7. Structure

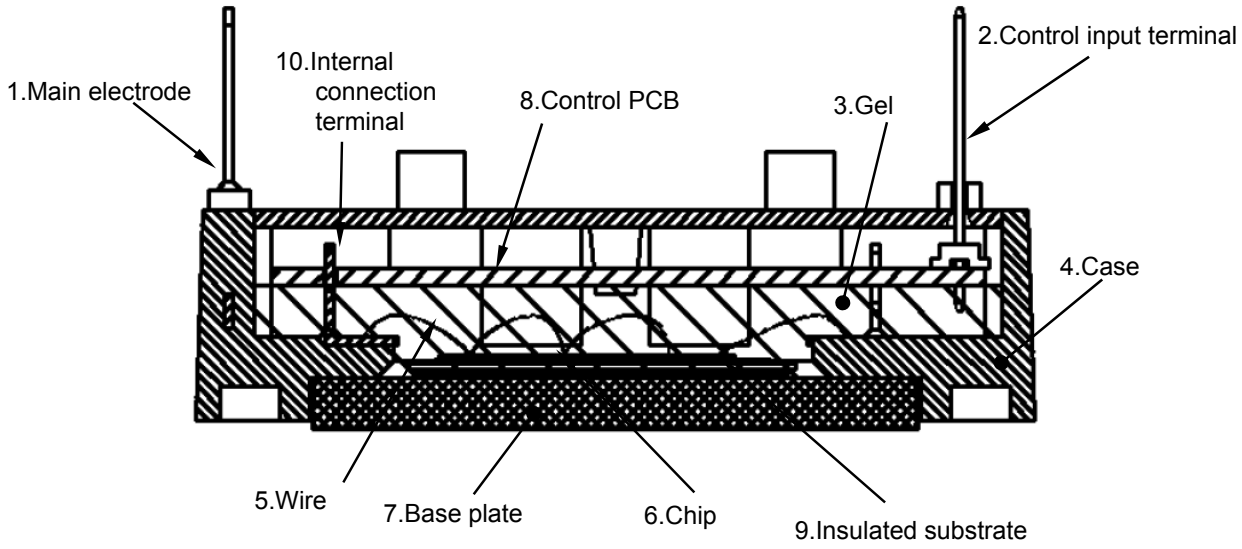
ex.) L1-series Small package Screw type



	Part	Quality of the material	UL Flame class
1	Main electrode	Copper plated with nickel	
2	Control input terminal	Brass plated with gold	
		PBT resin	UL 94-V0
3	Resin	Epoxy	UL 94-V0
4	Gel	Silicone	
5	Case	PPS resin	UL 94-V0
6	Wire	Aluminum	
7	Chip	Silicon	
8	Base plate	Copper	
9	Control PCB	Glass epoxy	UL 94-V0
10	Insulated substrate	Ceramic	
11	Internal connection terminal	Copper plated with nickel	

Note of Insulated substrate
IPM has UL(Underwriters Laboratories Inc) Yellow Card #80276 (file. #80271).

ex.) L1-series Mini package Screw type

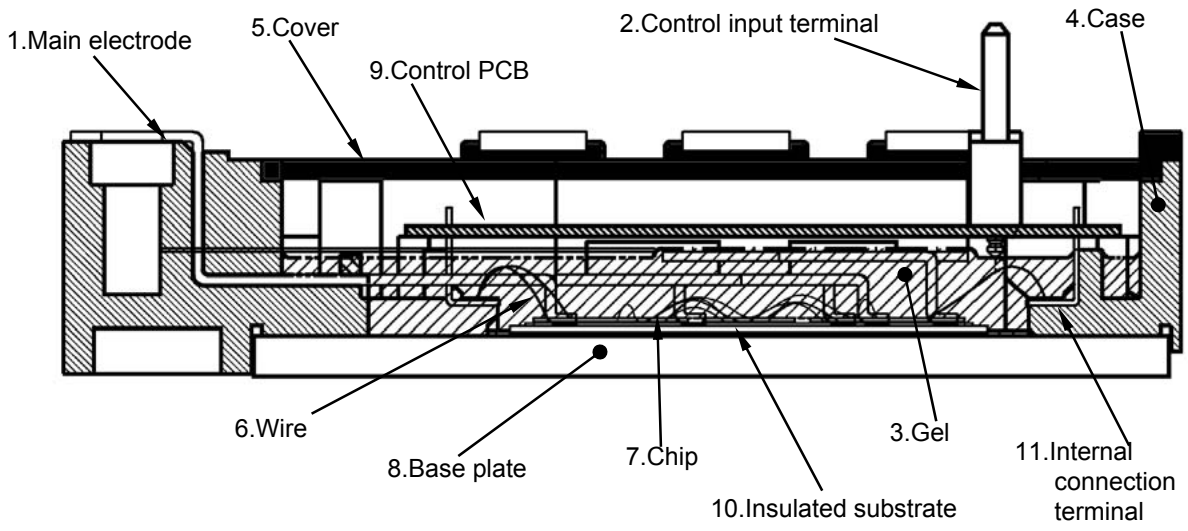


	Part	Quality of the material	UL Flame class
1	Main electrode	Copper plated with nickel	
2	Control input terminal	Brass plated with tin	
3	Gel	Silicone	
4	Case	PPS resin	UL 94-V0
5	Wire	Aluminum	
6	Chip	Silicon	
7	Base plate	Copper	
8	Control PCB	Glass epoxy	UL 94-V0
9	Insulated substrate	Ceramic	
10	Internal connection terminal	Copper plated with nickel	

Note of Insulated substrate

IPM has UL(Underwriters Laboratories Inc) Yellow Card #80276 (file. #80271).

ex.) L1-series Medium package

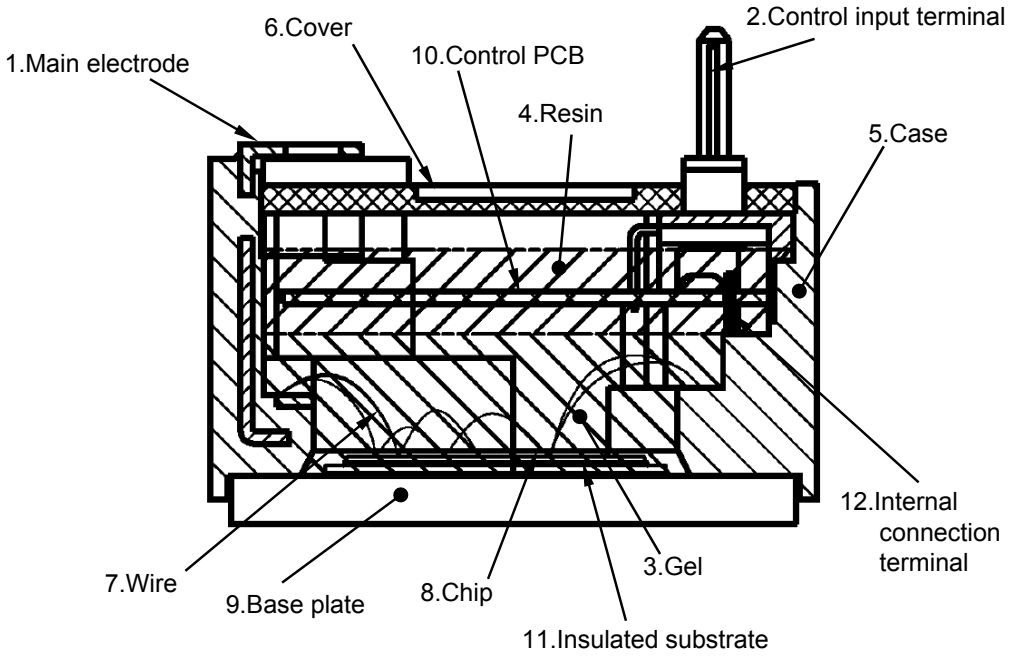


	Part	Quality of the material	UL Flame class
1	Main electrode	Copper plated with nickel	
2	Control input terminal	Brass plated with gold	
		PBT resin	UL 94-V0
3	Gel	Silicone	
4	Case	PPS resin	UL 94-V0
5	Cover	PPS resin	UL 94-V0
6	Wire	Aluminum	
7	Chip	Silicon	
8	Base plate	Copper	
9	Control PCB	Glass epoxy	UL 94-V0
10	Insulated substrate	Ceramic	
11	Internal connection terminal	Copper plated with nickel	

Note of Insulated substrate

IPM has UL(Underwriters Laboratories Inc) Yellow Card #80276 (file. #80271).

ex.) S1-series package



	Part	Quality of the material	UL Flame class
1	Main electrode	Copper plated with nickel	
2	Control input terminal	Brass plated with gold	
		PBT resin	UL 94-V0
3	Gel	Silicone	
4	Resin	Epoxy	UL 94-V0
5	Case	PPS resin	UL 94-V0
6	Cover	PPS resin	UL 94-V0
7	Wire	Aluminum	
8	Chip	Silicon	
9	Base plate	Copper	
10	Control PCB	Glass epoxy	UL 94-V0
11	Insulated substrate	Ceramic	
12	Internal connection terminal	Copper plated with nickel	

Note of Insulated substrate

IPM has UL(Underwriters Laboratories Inc) Yellow Card #80276 (file. #80271).

8. Correct and Safety Use of Power Module

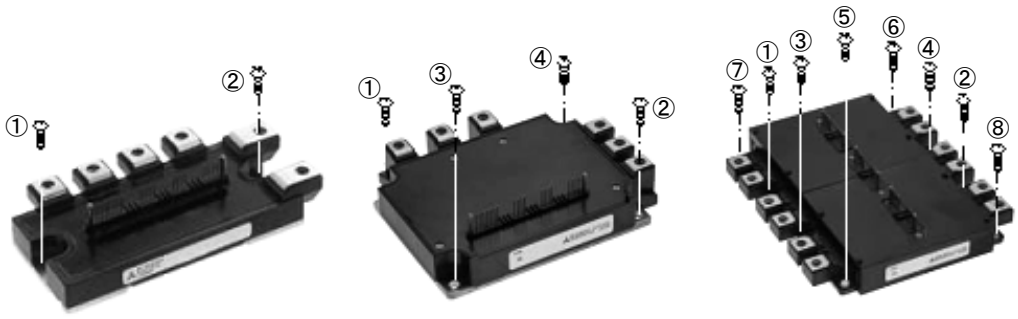
Unsuitable operation (such as electrical, mechanical stress and so on) may lead to damage of power modules.
Please pay attention to the following descriptions and use Mitsubishi Electric's IGBT modules according to the guidance.

	⚠ Cautions
During Transit	• Keep sipping cartons right side up. If stress is applied by either placing a carton upside down or by leaning a box against something, terminals can be bent and/or resin packages can be damaged. • Tossing or dropping of a carton may damage devices inside. • If a device gets wet with water, malfunctioning and failure may result. Special care should be taken during rain or snow to prevent the devices from getting wet.
Storage	• The temperature and humidity of the storage place should be 5~35°C and 45~75% respectively. The performance and reliability of devices may be jeopardized if devices are stored in an environment far above or below the range indicated above.
Prolonged Storage	• When storing devices more than one year, dehumidifying measures should be provided for the storage place. When using devices after a long period of storage, make sure to check the exterior of the devices is free from scratches, dirt, rust, and so on.
Operating Environment	• Devices should not be exposed to water, organic solvents, corrosive gases, explosive gases, fine particles, or corrosive agents, since any of those can lead to a serious accident.
Flame Resistance	• Although the epoxy resin and case materials are in conformity with UL 94-V0 standards, it should be noted that those are not non-flammable.
Anti-electrostatic Measures	(1) Precautions against the device rupture caused by static electricity Static electricity of human bodies and cartons and/or excessive voltage applied across the gate to emitter may damage and rupture devices. The basis of anti-electro static build-up and quick dissipation of the charged electricity. * Containers that are susceptible to static electricity should not be used for transit nor for storage. * Gate to emitter should be always shorted with a carbon cloth or the like until right before a module is used. Never touch the gate terminals with bare hands.
Anti-electrostatic Measures	* Always ground the equipment and your body during installation (after removing a carbon cloth or the like. It is advisable to cover the workstation and it's surrounding floor with conductive mats and ground them. * It should be noted that devices may get damaged by the static electricity charged to a printed circuit board if the gate to emitter of the circuit board is open. * Use soldering irons with grounded tips. (2) Precautions when the gate to emitter is open * Voltage should not be applied across the collector to emitter when the gate to emitter is open. * The gate to emitter should be shorted before removing a device from a unit.

⚠ Cautions

Mounting

When mounting a module on a heat sink, a device could get damage or degrade if a sudden torque ("one side tightening ") is applied at only one mounting terminal, since stress is applied on a ceramic plate and silicon chips inside the module. Shown in following figure is the recommended torquing order for mounting screws.



a) Two point mounting type b) four point mounting type c) eight point mounting type

Temporary tightening :①→②	①→②→③→④	①→②→③→④→⑤→⑥→⑦→⑧
Final tightening :②→①	④→③→②→①	①→②→③→④→⑤→⑥→⑦→⑧

The recommended torquing order for mounting screws

*:Temporary tightening torque should be set at 20~30% of maximum rating.

Also, care must be taken to achieve maximum contact (i.e. minimum contact thermal resistance) for the best heat dissipation.)

The flatness of a heat sink where a module is mounted (ref. following figure) should be as follows. Also, the surface finish should be less than Rz12s.

Copper base plate module:−100μm~+100μm

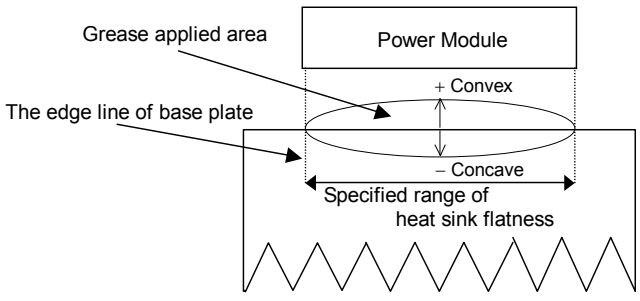
Thermal compound with good thermal conductivity should be applied evenly about Aluminum base plate modules:−100μm~+200μm on the contact surface of a module and a heat sink.

Heat sink flatness: Less than ± 20 micrometers on a length of 100mm
/Less than 10 micrometers of roughness

Thermal grease thickness: +50~+100μm

Grease on the contact surface prevents the corrosion of the contact surface. However, use the kind of grease that has a stable characteristic over the whole operating temperature range and does not change its properties for several years.

A torque wrench shall be used in tightening mounting screws and tighten screws to the specified torque. Excessive torquing may result in damage or degradation of a device.



Heat Sink Flatness

9.Reliability

Please refer to the URL of our web site. “http://www.mitsubishichips.com/Global/index.html”

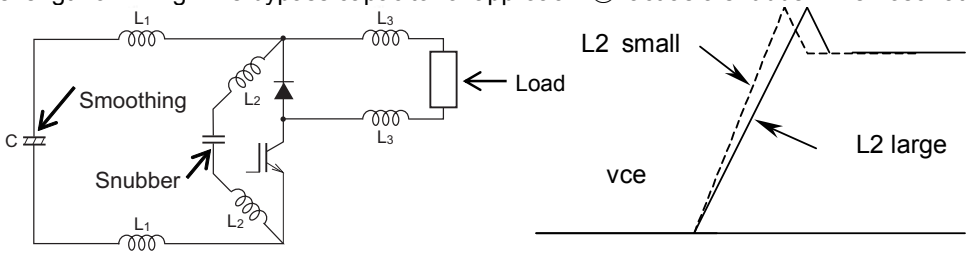
10. Installation of power Module

10-1. Installing Capacitor

During switching, voltage is induced in power circuit stray inductance by the high di/dt of the main current. This voltage can appear on the IPM and cause damage. In order to avoid this problem, guidelines that should be followed in designing the circuit layout are:

① Located the smoothing capacitor as close as possible to the IPM
② Use ceramic capacitor near the IPM to bypass high frequency current
③ Adopt low impedance electrolytic capacitor as smoothing capacitor
④ Use snubber circuit to absorb surge voltage
⑤ Decrease switching speed in order to lower di/dt.

② and ⑤ are the most effective to reduce surge voltage. The stray inductance of snubber circuit generally is not considered to avoid complicating the circuit. In addition, combination of ②, ④, ⑤ is needed since there is a limit on the length of wiring. The bypass capacitor of approach ② act as a snubber when oscillation is occurring.



L1 : Stray inductance between the electrolytic capacitor and the IPM.
L2 : Stray inductance between the filter capacitor and the driver.
L3 : Stray inductance between the load and the power circuit's output stage

10-2. Installation Hints

When mounting IPM on a heat-sink, uneven mounting can cause the modules ceramic isolation to crack. To achieve the best thermal radiation effect, the bigger the contact area is, the smaller the thermal resistance is. Heat-sink should have a surface finish in range of Rz6 ~ Rz12, curvature within 100μm.

Uniform coating of thermal grease between the module and heat-sink can prevent corrosion of contact parts. Select a compound, which has stable characteristics over the whole operating temperature range and does not change its properties over the life of the equipment.

Use a uniform coating of thermal interface compound. The thickness of thermal grease should be ranked in 100~200μm according to the surface finish.

Mounting screws should be tightened by using a torque wrench to the prescribed torque in progressive stages in a cross pattern. As mentioned before, over torque terminal or mounting screws may result in damage of IPM.

When an electric driver is used, thermal grease with low viscosity is recommended and extra grease must be extruded before final tightening screws.

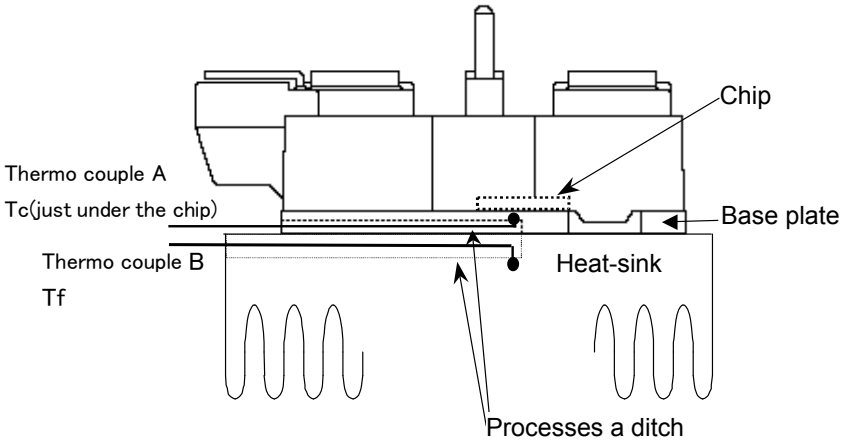
* For the recommended torque order for mounting screws referring to "Installation Method" in the section of
"Correct and Safety Use of Power Module"

Note) Maximum torque specifications are provided in device data sheets. The type and quantity of thermal compounds having an effect on the thermal resistance are determined by consideration of both thermal grease and heat-sink. Typical value given in datasheet is measured by using thermal grease produced by Shin-Etsu Chemical Co.,Ltd.
(G-746, which has not issued in Shin-Etsu's publications, is almost the same as G-747.)

10-3. Thermal Impedance Considerations & Chip Layout

The junction to case thermal resistance $R_{th(j-c)}$ and the case to heat-sink thermal resistance $R_{th(c-f)}$ are given in datasheet.

The case temperature has been measured at the just under the chip. The chip location is given with a data sheet.



·Note

*The thermal impedance depends on the material, area and thickness of heat-sink. The smaller the area and the thinner the heat-sink is, the lower the impedance is for the same material.

*The type and quantity of thermal compounds can affect the thermal resistance.

Thermal resistance of IPM L1-series

Thermal resistance 600V type

Type Name	Inverter part Just under the chip		Brake part Just under the chip		contact thermal resistance
	IGBT-chip Rth(j-c)Q	FWDi-chip Rth(j-c)	IGBT-chip Rth(j-c)Q	FWDi(P)-chip Rth(j-c)	Rth(c-f)
PM50RL1C060	0.74	1.28	0.74	1.28	0.085
PM50RL1A060, PM50RL1B060	0.44	0.75	0.44	0.75	0.038
PM50CL1A060, PM50CL1B060	0.44	0.75	-	-	0.038
PM75RL1A060, PM75RL1B060	0.37	0.63	0.44	0.75	0.038
PM75CL1A060, PM75CL1B060	0.37	0.63	-	-	0.038
PM100RL1A060, PM100RL1B060	0.32	0.52	0.44	0.75	0.038
PM100CL1A060, PM100CL1B060	0.32	0.52	-	-	0.038
PM150RL1A060, PM150RL1B060	0.25	0.41	0.38	0.64	0.038
PM150CL1A060, PM150CL1B060	0.25	0.41	-	-	0.038
PM200RL1A060	0.20	0.30	0.32	0.53	0.023
PM200CL1A060	0.20	0.30	-	-	0.023
PM300RL1A060	0.15	0.23	0.24	0.39	0.023
PM300CL1A060	0.15	0.23	-	-	0.023

Thermal resistance 1200V type

Type Name	Inverter part		Brake part		contact thermal resistance
	Just under the chip		Just under the chip		
	IGBT-chip Rth(j-c)Q	FWDi-chip Rth(j-c)	IGBT-chip Rth(j-c)Q	FWDi(P)-chip Rth(j-c)	Rth(c-f)
PM25RL1C120	0.70	1.18	0.70	1.18	0.085
PM25RL1A120,PM25RL1B120	0.97	1.60	0.97	1.60	0.038
PM25CL1A120,PM25CL1B120	0.97	1.60	-	-	0.038
PM50RL1A120,PM50RL1B120	0.27	0.47	0.39	0.67	0.038
PM50CL1A120,PM50CL1B120	0.27	0.47	-	-	0.038
PM75RL1A120,PM75RL1B120	0.21	0.36	0.27	0.47	0.038
PM75CL1A120,PM75CL1B120	0.21	0.36	-	-	0.038
PM100RL1A120	0.19	0.31	0.28	0.48	0.023
PM100CL1A120	0.19	0.31	-	-	0.023
PM150RL1A120	0.15	0.23	0.21	0.36	0.023
PM150CL1A120	0.15	0.23	-	-	0.023

Thermal resistance of IPM S1-series

Thermal resistance 600V type

Type Name	Inverter part		contact thermal resistance
	Just under the chip		
	IGBT-chip Rth(j-c)Q	FWDi-chip Rth(j-c)	Rth(c-f)
PM50CS1D060	0.40	0.68	0.046
PM75CS1D060	0.33	0.55	0.046
PM100CS1D060	0.28	0.46	0.046
PM150CS1D060	0.21	0.35	0.046
PM200CS1D060	0.18	0.27	0.046

Thermal resistance 1200V type

Type Name	Inverter part		contact thermal resistance
	Just under the chip		
	IGBT-chip Rth(j-c)Q	FWDi-chip Rth(j-c)	Rth(c-f)
PM25CS1D120	0.37	0.59	0.046
PM50CS1D120	0.25	0.41	0.046
PM75CS1D120	0.20	0.32	0.046
PM100CS1D120	0.18	0.27	0.046

10-4. Coating Method of Thermal Grease (Example)

The coating method of thermal grease is introduced in this section. The thermal grease is called as grease in the following.

① Preparations: power module, grease, scraper or roller, electronic mass meter and gloves

② Relationship between the coating amount and thickness is,

$$\text{Thickness of grease} = \frac{\text{amount of grease}\,[\text{g}]}{\text{base area of module}\,[\text{cm}^2] \times \text{density of grease}\,[\text{g/cm}^3]}$$

The recommended thickness of grease is 100μm~200μm.
The amount of grease can be obtained as the following example.

For example : For case with size of 110×89(PM100CSD060), the amount of Shin-Etsu Chemical Co.,Ltd. grease G-746 can be calculated through the equation below.

$$100 \sim 200\mu\text{m} = \frac{\text{amount of grease}\,[\text{g}]}{97.9[\text{cm}^2] \times 2.66[\text{g/cm}^3]}$$

$\therefore$The amount needed is$\fallingdotseq$2.6~5.2 [g]

③ Measure the mass of module

④ Measure the grease with the same amount as calculated

⑤ Coating the module base uniformly by using scraper or roller

⑥ Mask print of grease.

Finally it is fulfilled to uniformly cover thermal grease on the module base with specified thickness.

Thermal Compounds

Manufacturer	Type	Note
Shin-Etsu Chemical Co., Ltd. Momentive Performance Materials	KS-613, G-747, else YG6260, YG6260V	
ALCAN	UNIVERSAL JOINTING-COMPOUND	For non-insulation type

For more information, please refer to manufacturers.

ALCAN UNIVERSAL JOINTING-COMPOUND is grease for the aluminum conductor connection.
The purpose of grease is electricity and a contact resistance decline by the contact-ability improvement and the corrosion control of the aluminum surface.
It seems that there is long-range use experience but because we are not the one of the purpose to improve a heat conduction at the contacted part, the contact thermal resistance reductional effect cannot look forward to it too much. When employing these, the more enough radiation design becomes necessary.

10-5. Connecting the Interface circuit

The input pins of Mitsubishi Intelligent Power Modules are design to be connected directly to a printed circuit board. Noise pick up can be minimized by building the interface circuit on the PCB near the input pins of the module. L1B,L1C type modules have tin plated control and power pins that are designed to be soldered directly to the PCB. L1A, S1D type modules have gold plated pins that are design to be connected to the PCB using an inverse mounted header receptacle. It is the special connector of IPM which secured an electrical clearance among the terminals (U-V, V-W, W-U of P-side and N). The terminal with gold plate is recommended from the viewpoint of contact reliability.

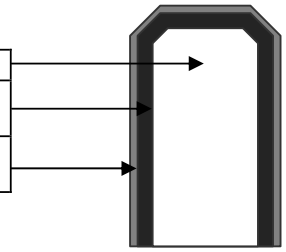
IPM type	Connection method and type name of connector
PM50RL1C060 PM25RL1C120 PM50RL1B060, PM50CL1B060 PM75RL1B060, PM75CL1B060 PM100RL1B060, PM100CL1B060 PM150RL1B060, PM150CL1B060 PM25RL1B120, PM25CL1B120 PM50RL1B120, PM50CL1B120 PM75RL1B120, PM75CL1B120	Main terminal Connect by solder. Control terminal Connect by solder.
PM50RL1A060, PM50CL1A060 PM75RL1A060, PM75CL1A060 PM100RL1A060, PM100CL1A060 PM150RL1A060, PM150CL1A060 PM200RL1A060, PM200CL1A060 PM300RL1A060, PM300CL1A060 PM25RL1A120, PM25CL1A120 PM50RL1A120, PM50CL1A120 PM75RL1A120, PM75CL1A120 PM100RL1A120, PM100CL1A120 PM150RL1A120, PM150CL1A120	Main terminal Connect by screw (screw:M5). Control terminal Connect by connector. **DF10-31S-2DSA(68), or DF10-31S-2DSA(62)** (HIROSE ELECTRIC CO., LTD)
PM50CS1D060, PM75CS1D060 PM100CS1D060, PM150CS1D060 PM200CS1D060 PM25CS1D120, PM50CS1D120 PM75CS1D120, PM100CS1D120	Main terminal Connect by screw (screw:M4). Control terminal Connect by connector. **MDF7-25S-2.54DSA(31), or MDF7-25S-2.54DSA(32)** (HIROSE ELECTRIC CO., LTD)

10-6. Terminal of IPM

(1) The material of control terminal of IPM (L1-series RL1A, CL1A type /S1-series)

As a reference of the connector selection, the material and the metal finishing of the control terminal on the side of IPM are shown below.

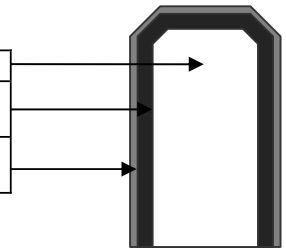
Main material		Brass
The specification of the plating	Substrate	Nickel (Ni) thickness= 1 ~ 5 um
	Surface	Gold (Au) thickness= 0.05 ~ 0.2 um



(2) The material of control terminal of IPM (L1-series RL1B, CL1B type)

As a reference of the connector selection, the material and the metal finishing of the control terminal on the side of IPM are shown below.

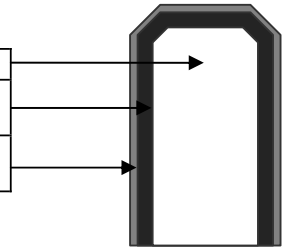
Main material		Brass
The specification of the plating	Substrate	Nickel (Ni) thickness= 1 ~ 6 um
	Surface	Tin (Sn) thickness= 4 ~ 10 um



(3) The material of control terminal of IPM (L1-series RL1C type)

As a reference of the connector selection, the material and the metal finishing of the control terminal on the side of IPM are shown below.

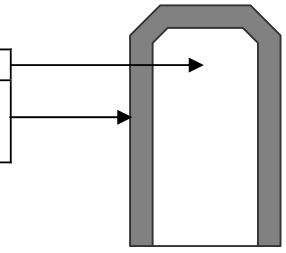
Main material		Brass
The specification of the plating	Substrate	Nickel (Ni) thickness= 0.5 ~ 1 um
	Surface	Tin (Sn) thickness= 2 ~ 6 um



(4) The material of main terminal of IPM

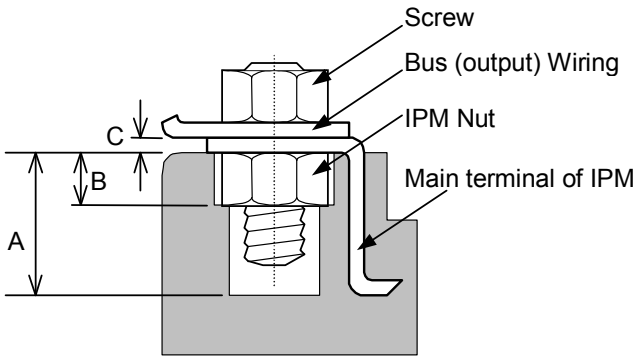
As a reference of the connector selection, the material and the metal finishing of the main terminal on the side of IPM are shown below.

Main material		Copper
The specification of the plating	Surface	Nickel (Ni) thickness= 2 ~ 6 um



(5) The main terminal of IPM

The structure of main terminal of IPM are shown bellow.



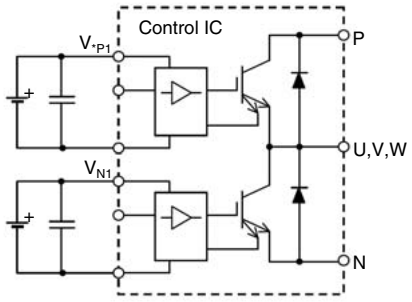
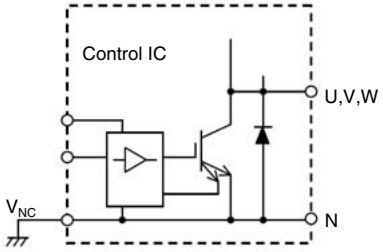
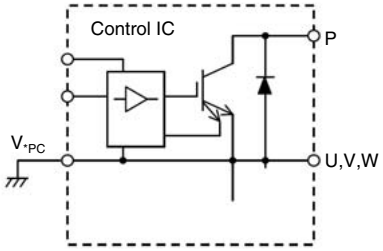
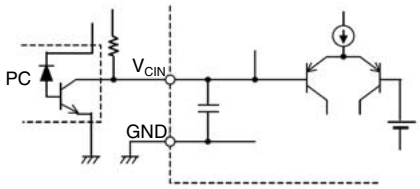
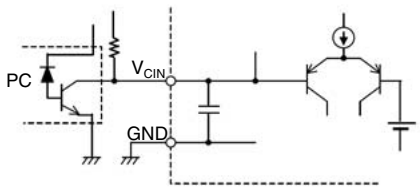
Package	Screw	Deepness of Screw Hole Mark A (mm)	Thickness of IPM Nut Mark B (mm)	Thickness of Main Terminal Mark C (mm)
L1-series RL1A/CL1A	M5	Typ. 9.5/ min. 9.0	Typ. 4.0	Typ. 0.8
S1-series	M4	Typ. 6.5/ min. 6.0	Typ. 3.3	Typ. 0.8

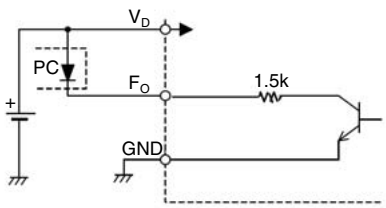
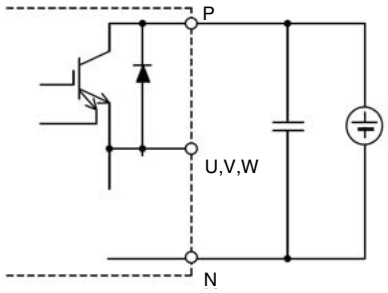
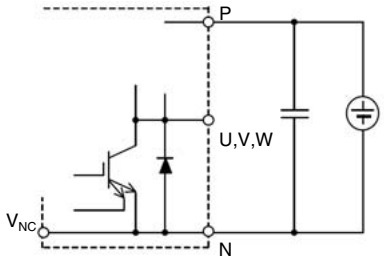
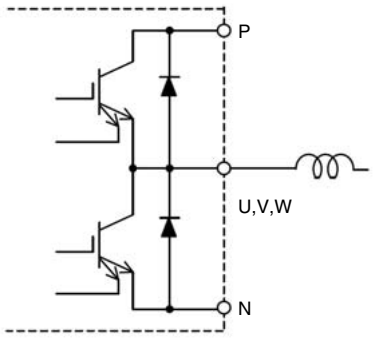
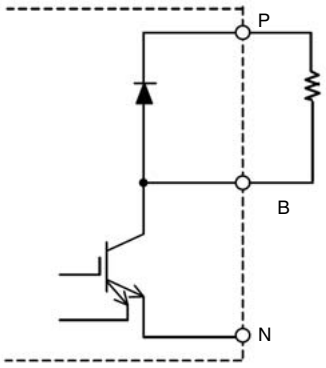
(6) The guide pin of IPM

The guide pin on both sides of the control terminal of IPM is metal. The guide pin is molded by plastic, and isolated.

11. Using IPM

11-1. Instruction of the symbol of a terminal of IPM

No	Name	Symbol	Equivalent Circuit	Operation (description)
1	Power -supply	V_D V_{UP1} V_{VP1} V_{WP1}		Power supply terminals for control IC and driving IGBT. Supply power commonly to lower arms and individual, insulated power to upper arms. For 6in1 and 7in1 types, 4 independent power supplies are required; three to upper arms and one to lower arm. UV lock-out functions if power is 12.5VDC or lower. Control signals are not effective for operation under this condition. Fo signal is output. If power is 16.5VDC or higher, operation is not guaranteed under short circuit condition. This is due to IGBT gate characteristics. Typical value is 15VDC. In order to prevent malfunction caused by noise and ripples in supply voltage, connect a smoothing capacitor of favorable frequency characteristics very close to IC terminals.
2	Ground	V_{NC}		Ground for reference power supply for lower arms. This ground is common to each of three phase for 6- or 7-element types. This is also the ground of control power supply. Bus line current should not be allowed to flow through this terminal to avoid noise influences. PCB pattern should not be such that connects this terminal and N. This terminal is internally connected to inverter ground N. Difference in electric potential between N and VNC may occur in practical operation.
		V_{UPC} V_{VPC} V_{WPC}		Grounds for reference power supply for upper arm of each phase. Lower power supply impedance as much as possible for greater resistance to noise. Insulate each phase of U, V and W.
3	Control -signal	U_P V_P W_P U_N V_N W_N		Input terminals for controlling IPM switching operation. Operates by voltage input signals. Internally connected to comparator. In usual applications, external pull-up resistor is connected to control power supply, and external opto-coupler for insulation purpose is also connected. As these terminals are susceptive of noise, design a shortest route in pattern layout and also take care for wiring. Connect a capacitor having good frequency characteristics between power supply and GND.
4	Brake Control -signal	Br		This terminal is used with R_{XX} series. The purpose of this terminal is to prevent increase in P-N voltage, which is caused by regenerative current produced when AC motor decelerates. In usual applications, external pull-up resistor is connected to control power supply, and external opto-coupler for insulation purpose is also connected. This terminal has the same structure as control signal terminals, accordingly are susceptive of noise. Take similar measures.

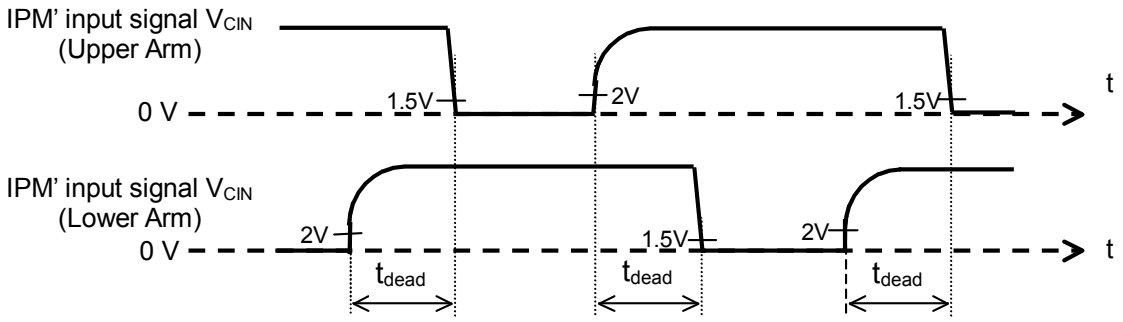
5	Fault -output	F_O		This is the output indicating faulty state of IPM. Faulty modes are classified into overheat, load (arm) short circuit, control power supply under voltage protection. This output does not make distinction of these modes, however. The terminal is an open collector with resistor connected in series. It is possible to directly insert a opto-coupler (or LED) between this terminal and V_D.
6	Inverter Power -supply	P		Power supply terminal to inverter. In usual applications, connect this terminal to positive (+) line after rectifying AC line. Internally connected to collector of upper arm IGBT. In order to suppress surge voltage caused by inductance component of PCB pattern, connect a smoothing capacitor very close to P and N terminals. It is also effective to add a film capacitor of good frequency characteristics.
7	Inverter -ground	N		Power supply ground of inverter. In usual applications, connect this terminal to ground (-) line after rectifying AC line. Make connection so that bus line current flows through this terminal. Internally connected to emitter of lower arm IGBT. This terminal is also connected to reference control ground V_{NC}. Difference in electric potential between VNC and N may occur in practical operation due to IPM's internal parasitic inductance.
8	Output	U V W		Inverter output terminal. A load such as AC motor is connected in usual applications. Take care for generation of surge voltage. Internally connected to mid point of IGBT modules (IPM) of half-bridge configuration.
9	Brake -output	B		This terminal is used with R_{XX} series. The purpose of this terminal is to prevent increase in P-N voltage, which is caused by regenerative current produced when AC motor decelerates. In usual applications, power dissipating resistor (brake resistor) is connected between this terminal and upper arm. Since this terminal is designed taking into account regenerative current produced when AC motor is decelerates, the current rating of this terminal is about 50% of that of IGBT chip used for U, V, and W. This terminal cannot endure use involving special control that allows a large current to flow.

11-2. Function of the IPM

Function	Symbol	Description
Drive	-	· Off-level input signal (V_{CIN} >$V_{CIN(off)}$) drives IGBT off, and on-level input signal (V_{CIN} <$V_{CIN(on)}$) drives IGBT on.
Short circuit Current Protection	SC	· IPM monitors forward collector current of each IGBT by current sensor built in IGBT chip. If the current exceeds SC trip level, IPM identifies it as short circuit and off the IGBT performing soft shutdown. · In case that an IGBT on lower arm have short-circuit, IPM turn off all lower IGBTs (U_N,V_N,W_N and Br) performing controlled shutdown. · IPM submits fault output if IGBT has short-circuit. The fault signal is output for the duration of t_{FO} when IPM detecting a short circuit state, reduces the gate voltage to halfway. · If there is no more short-circuit state while the input signal (V_{CIN}) is at off level, IPM resets itself from the short-circuit protection condition with the falling edge of the next input signal, and then the IGBT switching operation resets.
Over Temperature Protection	OT	· IPM monitors each IGBT chip surface temperature. If the temperature exceeds SC trip level, IPM identifies it as short circuit and off the IGBT performing soft shutdown. · IPM identified to be in over temperature state when the base plate temperature exceeds OT lever until it drops OT reset level. · IPM submits and holds on fault output of over temperature when OT trip level is exceeded and until the temperature falls to OT reset level. · If there is no more over temperature state with IGBT while the input signal (V_{CIN}) is at off level, IPM reset itself from the over temperature protection with the falling edge of the next input signal, and then the IGBT switching operation restarts.
Under-Voltage Lockout Protection	UV	· IPM monitors control power supply voltage of each arm. If the control power supply exceeds UV trip level and continues with it for a certain duration, IPM turns off IGBT, performing soft shutdown as long as the under voltage condition lasts. · In case of lower arm's UV operation, IPM turns off all lower arm's IGBTs (U_N, V_N, W_N and B), performing soft shutdown. · IPM identified to be in under voltage state when the control power supply voltage drops UV trip level until it goes up to UV reset level. · IPM submits and holds on fault output of under voltage after t_{dUV} until supply voltage returns to UV reset level. · If there is no more under voltage state with IGBT while the input signal (V_{CIN}) is at off level, IPM reset itself from the under voltage protection with the falling edge of the next input signal, and then the IGBT switching operation restarts.
Controlled Shutdown	-	· In all case of protective turn off operation, IPM reduces the IGBT's gate voltage gradually to final off level in order to reduce the turn-off surge voltage at large current-off.
Fault Output	F_O	· Fo terminal conducts to VNC terminal over 1ms when SC,OT or UV protection of lower arm is enabled. A resistor (1.5k) is connected inside IPM in series.

Dead time (tdead)

In order to prevent arm shoot through a dead time between high and low side input ON signals is required to be included in the system control logic. The tdead measured directly on the IPM input terminals



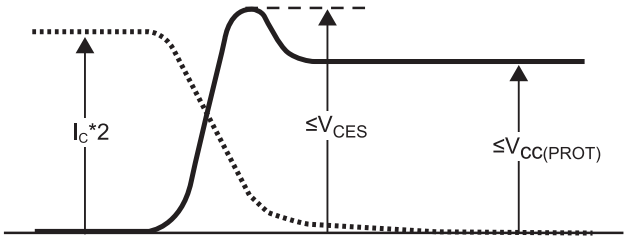
1.5V: Input on threshold voltage Vth(on) typical value, 2V: Input off threshold voltage Vth(off) typical value

11-3. Area of Safe Operation for Intelligent Power Modules

The IPMs built-in gate drive and protection circuits protect it from many of the operating modes that would violate the Safe Operation Area (SOA) of non-intelligent IGBT modules. A conventional SOA definition that characterizes all possible combinations of voltage, cur-rent, and time that would cause power device failure is not required. In order to define the SOA for IPMs, the power device capability and control circuit operation must both be considered. The resulting easy to use short circuit and switching SOA definitions for Intelligent Power Modules are summarized in this section.

(1) Switching SOA

Switching or turn-off SOA is normally defined in terms of the maximum allowable simultaneous volt-age and current during repetitive turn-off switching operations. In the case of the IPM the built-in gate drive eliminates many of the dangerous combinations of voltage and current that are caused by improper gate drive. In addition, the maximum operating current is limited by the over current protection circuit. Given these constraints the switching SOA can be defined using the waveform shown in following figure. This waveform shows that the IPM will operate safely as long as the DC bus voltage is below the data sheet VCC(prot) specification, the turn-off transient voltage across C-E terminals of each IPM switch is maintained below the VCES specification, Tj is less than 125°C, and the control power supply voltage is between 13.5V and 16.5V. In this waveform IOC is the maximum cur-rent that the IPM will allow without causing an Over Current (OC) fault to occur. In other words, it is just below the OC trip level. This waveform defines the worst case for hard turn-off operations because the IPM will initiate a controlled slow shutdown for currents higher than the OC trip level.

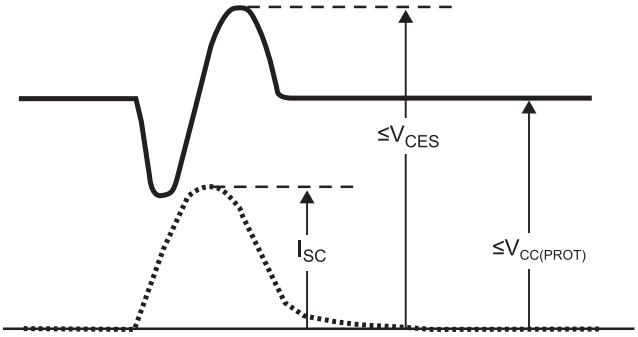


Switching SOA

(2) Short Circuit SOA

The waveform in following figure depicts typical short circuit operation. The standard test condition uses a minimum impedance short-circuit which causes the maximum short circuit current to flow in the device. In this test, the short circuit current (ISC) is limited only by the device characteristics. The IPM is guaranteed to survive non-repetitive short circuit and over current conditions as long as the initial DC bus volt-age is less than the VCC(prot)specification, all transient voltages across C-E terminals of each IPM switch are maintained less than the VCES specification, Tj is less than125°C, and the control supply volt-age is between 13.5V and 16.5V.The waveform shown depicts the controlled slow shutdown that is used by the IPM in order to help minimize transient voltages.

Note:
The condition VCE, VCES has to be carefully checked for each IPM switch. For easing the design an-other rating is given on the datasheets, VCC(surge), i.e., the maximum allowable switching surge voltage applied between the P and N terminals.



SC SOA

(3) Active Region SOA

Like most IGBTs, the IGBTs used in the IPM are not suitable for linear or active region operation. Normally device capabilities in this mode of operation are described in terms of FBSOA (Forward Biased Safe Operating Area). The IPM's internal gate drive forces the IGBT to operate with a gate voltage of either zero for the off state or the control supply voltage (VD) for the on state. The IPMs under-voltage lock out prevents any possibility of active or linear operation by automatically turning the power device off if VD drops to a level that could cause desaturation of the IGBT.

11-4. Fault Signal of IPM

IPM (Intelligent Power Modules) have sophisticated built-in protection circuits that prevent the power devices from being damaged should the system malfunction or be over stressed. Control supply under-voltage(UV), over temperature(OT), and short-circuit(SC) protection are all provided by the IPM's internal gate control circuits. A fault output signal is provided to alert the system controller if any of the protection circuits are activated. Following Fig9.7 is a block diagram showing the IPMs internally integrated functions.

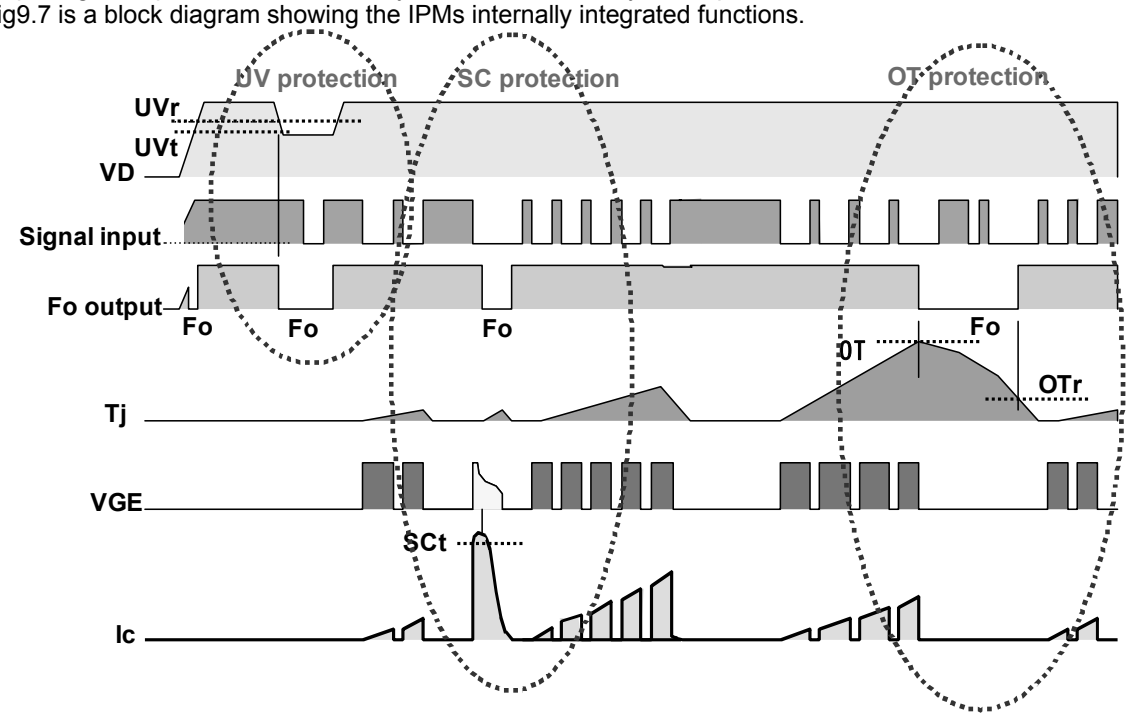


Fig.9.7 Timing chart of Control and protection of IPM

Control Supply Under-Voltage (UV)

The IPM's internal control circuits operate from an isolated 15V DC supply. If, for any reason, the voltage of this supply drops below the specified under-voltage trip level (UVt), the power devices will be turned off and a fault signal will be generated. Small glitches less than the specified tdUV(<10us) in length will not affect the operation of the control circuitry and will be ignored by the under voltage protection circuit. In order for normal operation to resume, the supply voltage must exceed the under voltage reset level (UVr). Operation of the under-voltage protection circuit will also occur during power up and power down of the control supply. This operation is normal and the system controller's program should take the fault output delay (tFo) into account.

Note)

1. Application of the main bus voltage at a rate greater than 20V/ms before the control power supply is on and stabilized may cause destruction of the power devices.
2. Voltage ripple on the control power supply with dv/dt in excess of 5V/us may cause a false trip of the UV lockout.

Over Temperature (OT)

The IPM has a temperature sensor mounted on surface of IGBT chips. If the temperature of the IGBT chips exceeds the over temperature trip level (OT) the IPMs internal control circuit will protect the power devices by disabling the gate drive and ignoring the control input signal until the over temperature condition has subsided. The fault output will remain as long as the over temperature condition exists. When the temperature falls below the over temperature reset level (OTr), and the control input is high (off-state) the power device will be enabled and normal operation will resume at the next low (on) input signal.

Note)

1. Tripping of the over-temperature protection is an indication of stressful operation. Repetitive tripping should be avoided.

Short Circuit (SC)

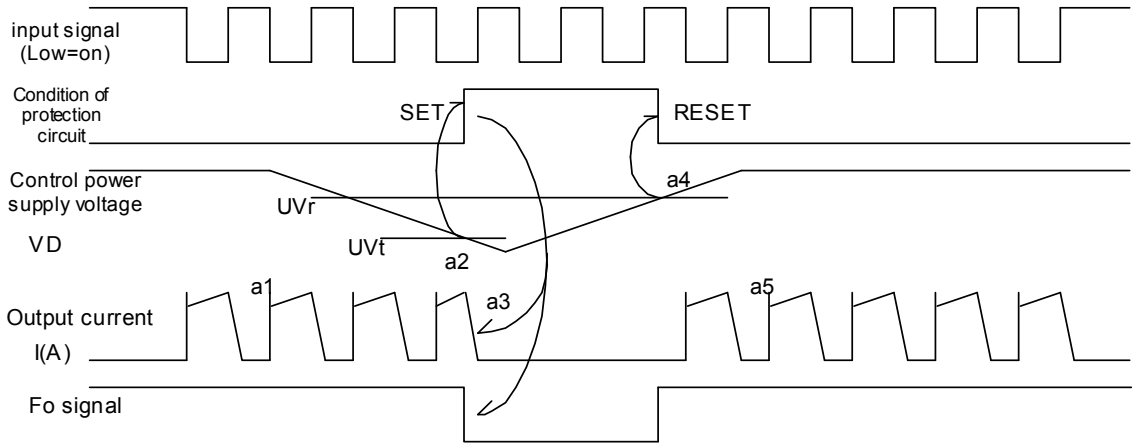
If a load short circuit occurs or the system controller malfunctions causing a shoot through, the IPMs built in short circuit protection will prevent the IGBTs from being damaged. When the current, through the IGBT exceeds the short circuit trip level (SC), an immediate controlled shutdown is initiated and a fault output is generated.

Note)

1. Tripping of the over current and short circuit protection indicates stressful operation of the IGBT. Repetitive tripping should be avoided.
2. High surge voltages may occur during emergency shutdown. Low inductance bus-work and snubbers are recommended.

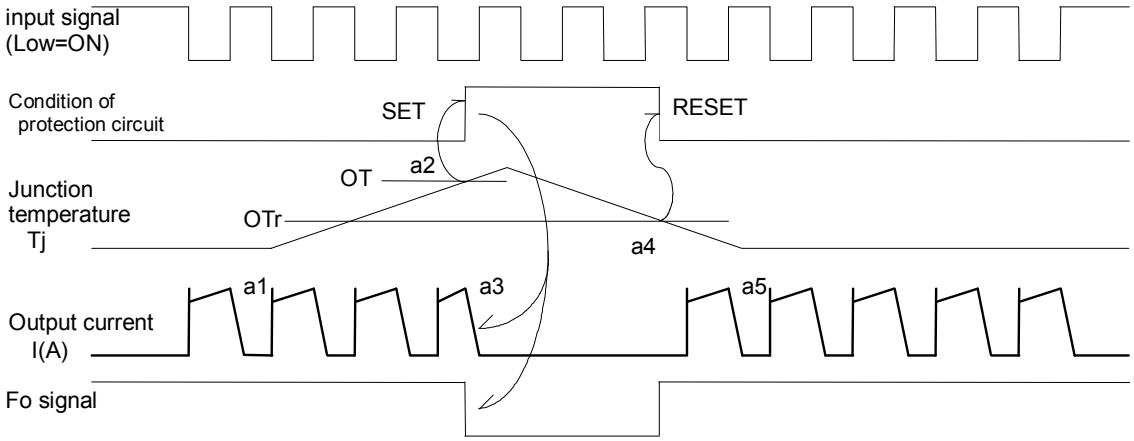
The operating-sequence of the UV protection

a1 : The normal operation=IGBT ON
a2 : The decline of control power supply voltage (UVt)
a3 : IGBT OFF (Even if the input signal is in on state)
a4 : The rise of control power supply (UVr)
a5 : The normal operation=IGBT ON



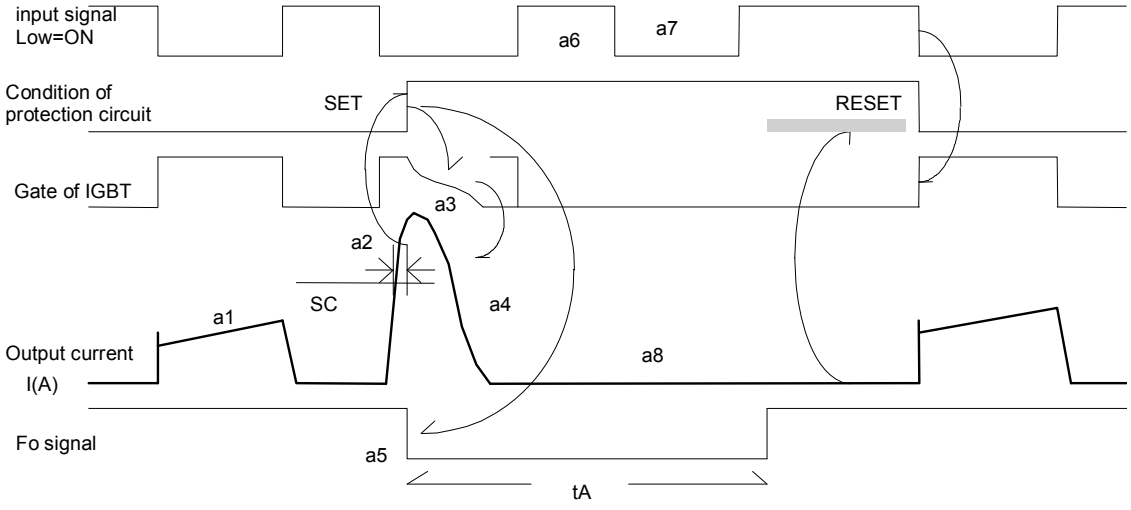
The operating-sequence of the OT protection

a1 : The normal operation=IGBT ON
a2 : The overheating detection (OTt)
a3 : IGBT OFF (Even if it makes an input signal to be on)
a4 : The overheating detection reset (OTr)
a5 : The normal operation=IGBT ON



The operating-sequence of the SC protection

a1 : The normal operation=IGBT ON
a2 : Short current detection (SCt)
a3 : IGBT gate is blocked softly.
a4 : IGBT turn off gradually.
a5 : Fo timer start (tFo=1.8ms typ.)
a6 : Input signal “H”=OFF
a7 : Input signal “L”=ON
a8 : IGBT maintains off. (When a6~a7 occurs at the time which is shorter than tA)



Although IPM has internal protection circuit, it is recommended to ensure the stress which exceeds a maximum rating does not happen repeatedly.
Therefore, if received Fo signal, please stop the control signal and stop the operation of IPM.
Because IPM doesn't exclude extraordinary cause, it has to be stopped by the system.

11-5. Interface Circuit Requirements

The IGBT power switches in the IPM are controlled by a low level input signal. The active low control input will keep the power devices off when it is held high. Typically the input pin of the IPM is pulled high with a resistor connected to the positive side of the control power supply. An on signal is then generated by pulling the control input low. The fault output is an open collector with its maximum sink cur-rent internally limited. When a fault condition occurs the open collector device turns on allowing the fault output to sink current from the positive side of the control supply. Fault and on/off control signals are usually transferred to and from the sys-tem controller using isolating inter-face circuits. Isolating interfaces allow high and low side control signals to be referenced to a common logic level. The isolation is usually provided by opto-couplers. However, fiber optics, pulse transformers, or level shifting circuits could be used. The most important consideration in interface circuit design is layout. Shielding and careful routing of printed circuit wiring is necessary in order to avoid coupling of dv/dt noise into control circuits. Parasitic capacitance between high side interface circuits, high and low side interface circuits, or primary and secondary sides of the isolating de-vices can cause noise problems. Careful layout of control power supply and isolating circuit wiring is necessary. The following is a list of guidelines that should be followed when designing interface circuits.

Interface Circuit layout Guidelines

a) Maintain maximum interface isolation. Avoid routing printed circuit board traces from primary and secondary sides of the isolation device near to or above and below each other. Any layout that increases the primary to secondary capacitance of the isolating interface can cause noise problems.

b) Maintain maximum control power supply isolation. Avoid routing printed circuit board traces from UP, VP, WP, and N-side supplies near to each other. High dv/dts exist between these supplies and noise will be coupled through parasitic capacitances. If isolated power supplies are derived from a common trans-former inter winding capacitance should be minimized.

c) Keep printed circuit board traces between the interface circuit and IPM short. Long traces have a tendency to pickup noise from other parts of the circuit.

d) Use recommended decoupling capacitors for power supplies and opto-couplers. Fast switching IGBT power circuits generate dv/dt and di/dt noise. Every precaution should be taken to protect the control circuits from coupled noise.

e) Use shielding. Printed circuit board shield layers are helpful for controlling coupled dv/dt noise.

f) High speed opto-couplers with high common mode rejection (CMR) should be used for signal input:
t_{PLH}, t_{PHL} < 0.8us
CMR > 10kV/s @ VCM = 1500V
Appropriate opto-coupler types are TLP-559(IGM), TLP-759(IGM) (TOSHIBA), HCPL-4506(AVAGO) and PS9613(NEC). Usually high-speed opto couple require a “0.1F” decoupling capacitor close to the opto coupler.

g) Select the control input pull up resistor with a low enough value to avoid noise pick-up by the high impedance IPM input and with a high enough value that the high speed opto transistor can still pull the IPM safely below the recommended maximum $V_{CIN(on)}$.

h) If some IPM switches are not used in actual application their control power supply must still be applied. The related signal input terminals should be pull up by resistors to the control power supply (VD) to keep the unused switches safely in off-state.

i) Unused fault outputs must be tied high in order to avoid noise pick up and unwanted activation of internal protection circuits. Unused fault outputs should be connected directly to the +15V of local isolated control power supply.

11-6. Control Power supply of IPM

(1) The control power supply
The control supply voltage range should be within the limits shown in the specifications.

Control supply voltage V_D(V)	Operation behavior
0~4.0	It is almost the same as no power supply. External noise may cause IPM malfunction (turns ON). Supply under-voltage protection will not operate and no Fo signal will be asserted.
4.0~12.5	Even if control input signals are applied, IGBT does not work Supply under-voltage protection starts operation and outputs Fo signals.
12.5~13.5	Switching operation works. However, this value is below the recommended one, $V_{CE(sat)}$ and switching time will be out of the specified values, it may increase collector dissipation and junction temperature.
13.5~16.5	Recommended values.
16.5~20	Switching operation works. This range, however, is over the recommended value, thus, too fast switching speed might cause the chips to be damaged
20.0~	The control circuit will be destroyed.

Specifications for Ripple Noise

High frequency noise super imposed on the control IC supply line might cause IC malfunction and cause an Fo signal output, and results IPM stop (interrupt gates). To avoid such malfunction, the supply circuit should be designed such that the noise fluctuation is smaller than +/- 5V/us, and the ripple voltage is less than 2V.

Specification: $\frac{dv}{dt} \le \pm 5V/us$, $Vripple \le 2Vp-p$

When the noise on the power supply line is a high frequency (pulse-width<about 50ns,pulse-vibration<about 5V) which does not cause an Fo output from IPM, the noise can be ignored.
The power supply should be a low impedance, be careful of the pattern layout.
Connect a bypass condenser with good frequency response and a smoothing condenser close to the terminals of IPM. It is effective for the prevention of the malfunction.

Control Supply Starting up and Shutting Down Sequence

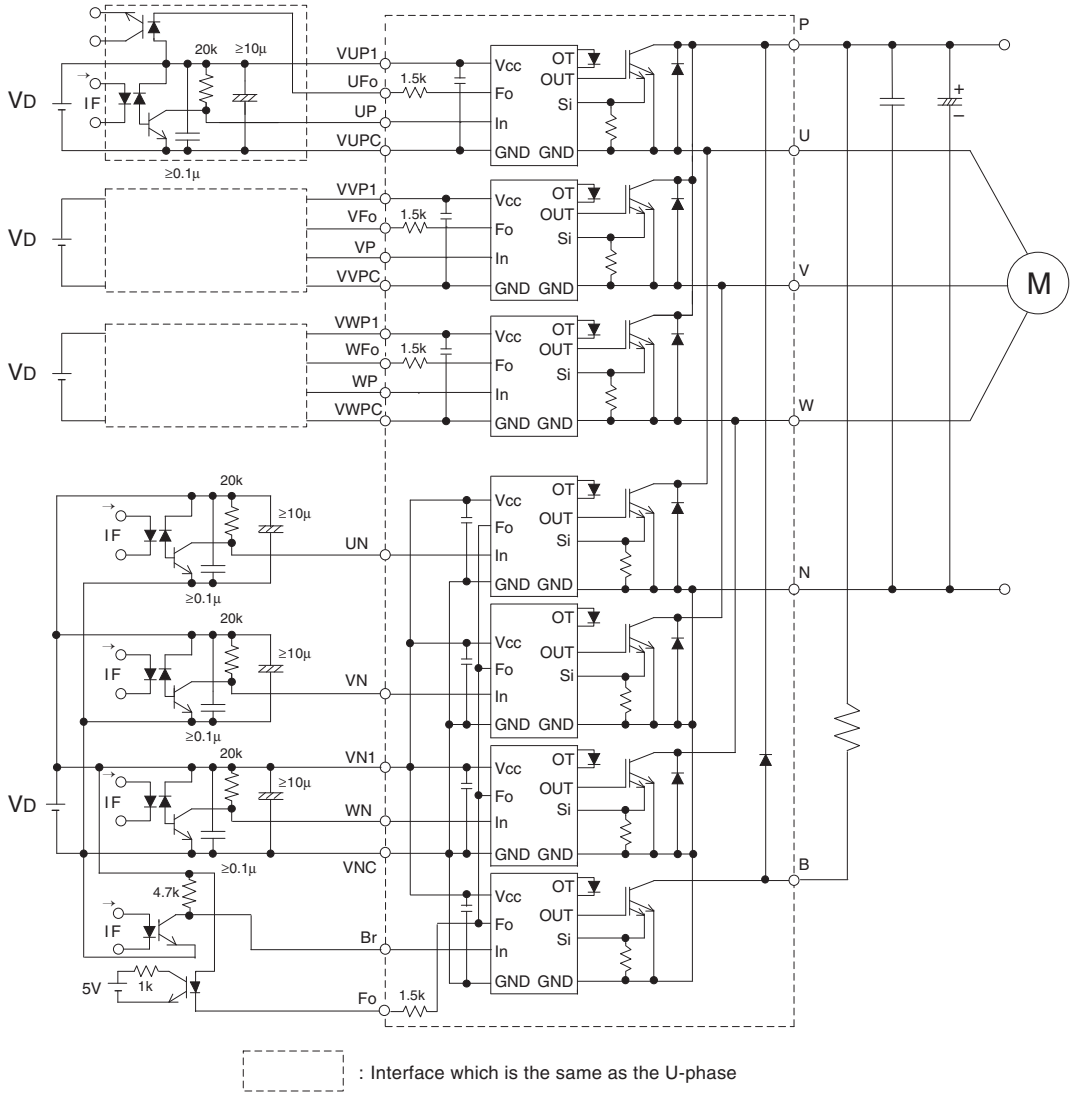
Control supply VD should be started up prior to the main supply (P-N supply).
Control supply VD should be shut down after the main supply (P-N supply).

If the main supply had been started up before the control supply, or if the main supply remains after control supply was shut down, external noise might cause the IPM malfunction.

As for the P-side, use the control power supply which was insulated in each of all of the 2 aspects.
As for the N-side , because the GND in 2 aspects and the converter part is common, a common power can be used for the three control sources in amount.

11-7. Applications of IPM L1/S1-series to Motor drive

(ex. 7in1 PM**RL1A060, PM**RL1A120)



Notes for stable and safe operation;

- Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto -coupler.
- Connect low impedance capacitor between the Vcc and GND terminal of each fast switching opto -coupler.
- Fast switching opto -couplers : tpLH, tpHL≦0.8 us, Use High CMR type.
- Slow switching opto -coupler : CTR＞100%
- Use 3 isolated control power supplies (V_D). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.
- Use line noise filter capacitor (ex. 4.7nF) between each input AC line and ground to reject common -mode noise from AC line and improve noise immunity of the system.

11-8. Interface of control side of IPM

IPM (Intelligent Power Modules) is easy to operate. The integrated drive and protection circuits require only an isolated power supply and a low level on/off control signal. A fault output is provided for monitoring the operation of the module internal protection circuits.

(1) Circuit and circuit constant of the IPM interface circuit

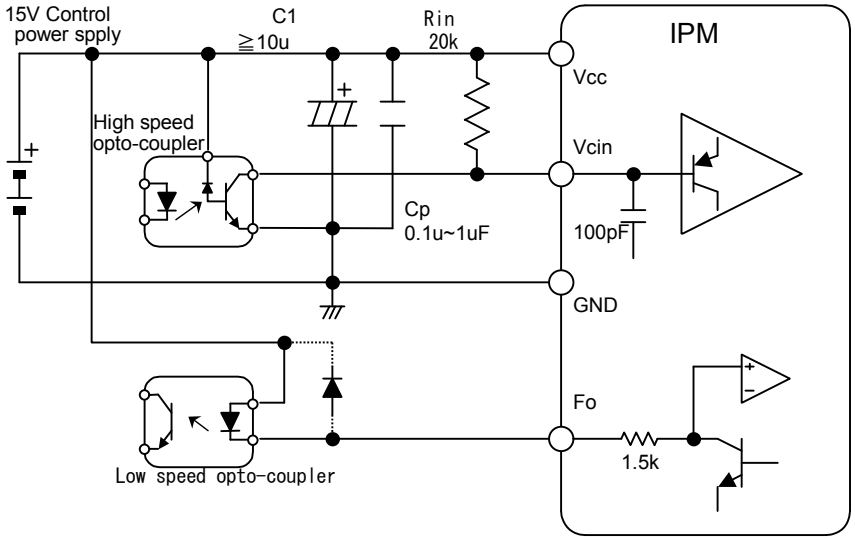
The parts of connecting IPM and controller (CPU) are required to use following parts.

- Input terminal (1) High speed opto-coupler, (2) Pull-up resistor
  (3) Condenser (Ceramic condenser for the ripple removal and electrolytic condenser for the power stabilization)
- Fo terminal (4) Low(high) speed opto-coupler
- Control power supply (5) The mutually insulated stabilized power source of +15 V
  (The negative power as it uses in IGBT-MOD is unnecessary.)

Example of constant value of the IPM interface circuit

Symbol	Name	Recommend Value	Note
Rin	Pull-up resistor	20kΩ	All input terminal (include Br)
C1	Smoothing capacitor	< 10uF	It is necessary that the charge and discharge electric current and the dv/dt electric current to IPM(IGBT gate) can be sufficiently absorbed.
Cp	Bypass condenser	< 0.1 ~ 1uF	
PC	Opto-coupler	High CMR, CTR	ex.) TLP-559(IGM), PS9613 etc

(2) IPM Internal circuit diagram and interface circuit



(3) IPM Control terminals

The IGBT power switches in the IPM are controlled by a low level input signal. The active low control input will keep the power devices off when it is held high. Typically the input pin of the IPM is pulled high with a resistor connected to the positive side of the control power supply. An ON signal is then generated by pulling the control input low.

The recommended value of the pull-up resistor is 20 kΩ but it can be smaller for the noise countermeasure and so on. However, if the pull-up resistor is set too small, it will affect the lifetime of the opto-coupler, please confirm the characteristics with lifetime and so on in the opto-coupler manufacturer.

The inside of the control input terminal is connected to the comparator and is with high impedance.

When IPM (IGBT) is turn-off , the output impedance of the opto-coupler becomes high. Total impedance of the circuit which connect the interface circuit is equal to a resistance of about 20KΩ.

(4) Example of opto coupler

The example of the opto-coupler recommended for IPM is shown below.

High speed opto coupler

High speed opto couplers are connected to the control input terminals of IPM.
When choosing opto coupler, pay attention to the parameters of response time (tpLH, tpHL) and CMR.
Choose the opto coupler that the value of tpLH, tPHL is less than 0.8us, and with high CMR.
Especially, ensure that the phenomena such as the ringing not occur.

For example)
PS9613 (NEC)
TLP559 (IGM), TLP759 (IGM) (Toshiba)
HCPL-4503, HCPL-4504, HCPL-4506 (Avogo TECHNOLOGIES)

The opto-coupler manufacturer sometimes has the IPM exclusive-goods (another form name) which sorted out a characteristic. Please inquire the opto-coupler of IPM compatible for the malfunction prevention when order.

Low speed opto coupler

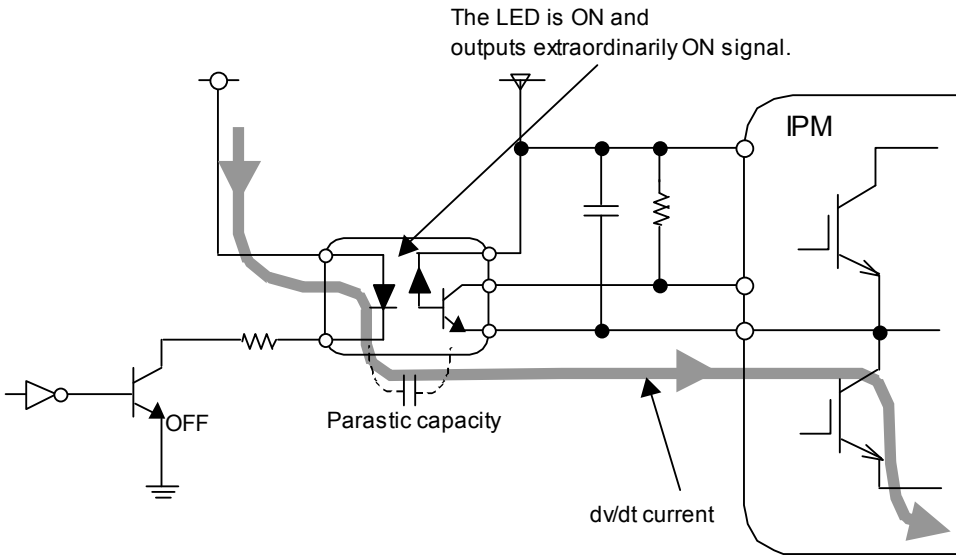
Low speed opto coupler is connected Fo terminal of IPM.
When choosing opto coupler, pay attention to the parameter of CTR.
Choose the opto coupler that the value of CTR is equal to or more than 100 %.

For example)
TLP-521 (Toshiba)
PS2502 (NEC)

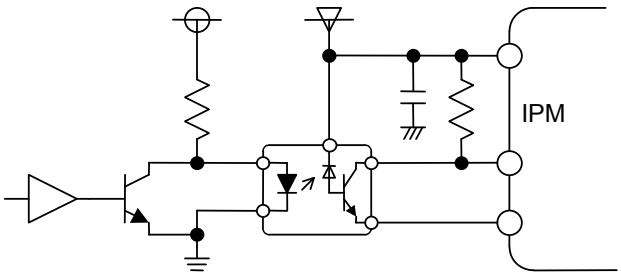
Please inquire the manufacturer that the opto-coupler has or has not problem when work under your environmental condition.

(5) Notice of using opto coupler

The opto coupler can isolate the primary side and secondary side. But, this is not correct at the high frequency. Because, opto coupler have a parasitic capacity between primary side and secondary side. When high dv/dt is impressed, the pulse electric current flows from the primary side to the secondary side via the parasitic capacity of opto coupler. This current sometimes turn on the opto coupler.
Therefore, it is important to design a circuit so that the LED will not turn on erroneously by this dv/dt.
When the input signal is OFF, make sure the circuit that the LED of primary side of opto coupler is with low-impedance.



The example of a circuitry which is not good



The example of the circuit to recommend

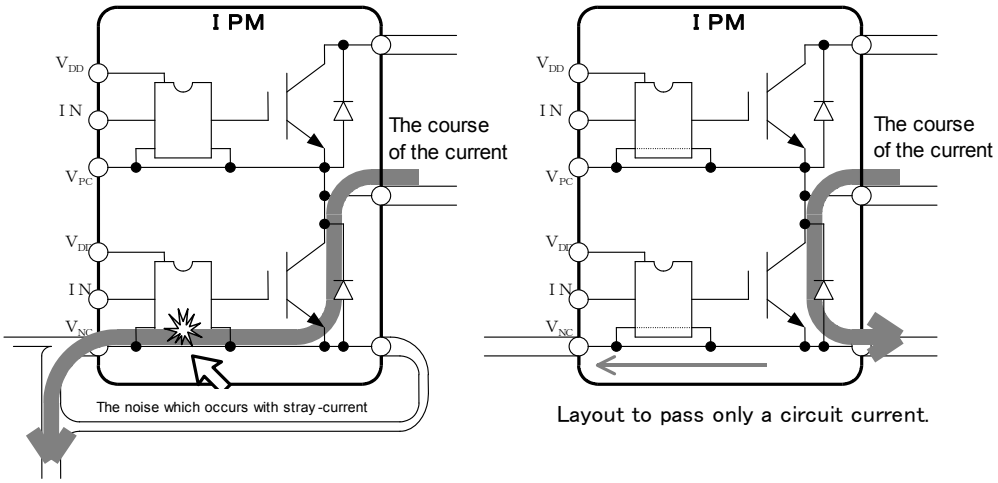
The recommended circuit doesn't make malfunction (LED of primary side of opto coupler is ON) because the dv/dt current can not turn ON the LED of primary side of opto coupler.

Please consult the application-note of the opto coupler for the detailed instruction of the circuit around the opto coupler.

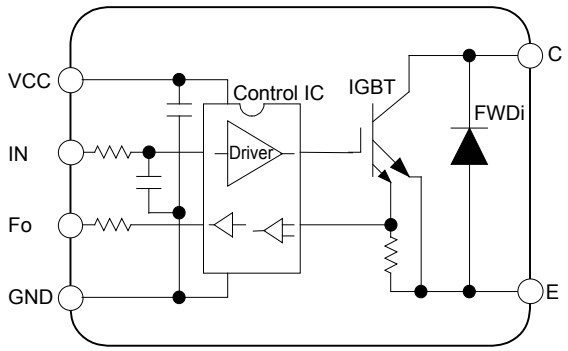
11-9. Other notice of using IPM

(1) The treatment of the terminal not to use
Type CL1A,CL1B have B terminal. These terminal aren't connected to the circuit. The pattern can be connected with this terminal. However, pay attention to the wiring. When connecting a pattern with these terminals, the noise might invades IPM via the terminals. Please just leave these terminals open.
If any phase of the IPM is not used, the corresponded control power supply in the circuit will not use. Please pull-up the corresponded input terminals and make IGBT off. This is to prevent the erroneous turn on of the circuit by noise.

(2) The connection of the control side GND(V_{NC}/V_{*PC}) and output emitter GND (N or U/V/W)
Do not connect the control side GND and the output emitter GND on the printed circuit board. Otherwise It will be easy to undergo influence by the noise. V_{NC} and the N terminal are connected inside IPM. If connecting VNC and N terminal, the current which should flow through N sometimes flows to VNC. Then, the electric potential difference occurs between N and VNC by parasitic inductance inside and might cause IC malfunction.



(3) The circuit structure inside
The IPM is built up with IGBT chip, FWDi chip, Control IC and the other discreet parts(R, C).
Gate of IGBT chip is MOS structure. However, The gate of IGBT chip doesn't directly connect to the control terminal of IPM. VD, Input, Fo and GND terminal are connected to the control IC. It is possible to consider the terminal of IPM to be a bipolar structure. The countermeasure against static electricity like conventional IC with MOS structure is unnecessary to IPM.
(The handling of IPM is equal to that of a bipolar IC.)



(4) The parallel operation
The IPM is not recommended for parallel operation.
Because the balance of the switching time and the current are not identical, the IPM with larger loss might be thermally damaged because it isn't possible to do the protection-coordination of each IPM.

11-10. The circuit current of control power supply of IPM

The circuit current of control power supply of IPM is shown below. This current is average of DC and fc=20kHz.

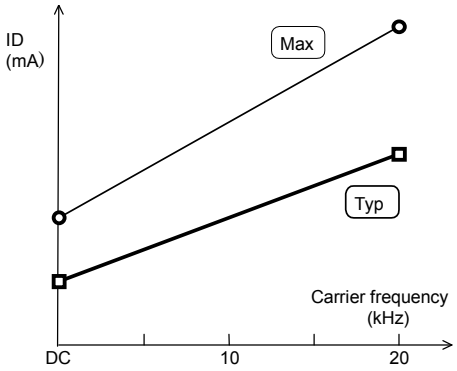
L1-series Condition : VD=15V,Tj=25°C, Unit : mA

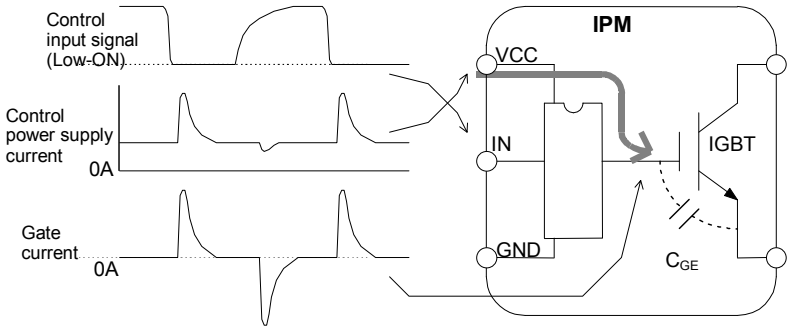
IPM L1-series	N-side				P-side (1 phase)			
	DC		20kHz		DC		20kHz	
Type. Name	Typ	Max	Typ	Max	Typ	Max	Typ	Max
PM50RL1C060	8	16	21	27	2	4	7	9
PM50RL1A/RL1B060	8	16	26	34	2	4	7	9
PM50CL1A/CL1B060	6	12	22	29	2	4	7	9
PM75RL1A/RL1B060	8	16	32	42	2	4	9	12
PM75CL1A/CL1B060	6	12	27	35	2	4	9	12
PM100RL1A060	8	16	37	48	2	4	11	14
PM100CL1A060	6	12	32	42	2	4	11	14
PM150RL1A060	8	16	51	66	2	4	14	18
PM150CL1A060	6	12	44	57	2	4	14	18
PM200RL1A060	8	16	75	98	2	4	20	26
PM200CL1A060	6	12	64	83	2	4	20	26
PM300RL1A060	8	16	99	129	2	4	25	33
PM300CL1A060	6	12	84	109	2	4	25	33
PM25RL1C120	8	16	25	33	2	4	9	12
PM25RL1A/RL1B120	8	16	32	42	2	4	9	12
PM25CL1A/CL1B120	6	12	27	35	2	4	9	12
PM50RL1A/RL1B120	8	16	50	65	2	4	14	18
PM50CL1A/CL1B120	6	12	43	56	2	4	14	18
PM75RL1A/RL1B120	8	16	70	91	2	4	19	25
PM75CL1A/CL1B120	6	12	59	77	2	4	19	25
PM100RL1A120	8	16	94	122	2	4	26	34
PM100CL1A120	6	12	80	104	2	4	26	34
PM150RL1A120	8	16	132	172	2	4	33	43
PM150CL1A120	6	12	115	150	2	4	33	43

S1-series Condition : VD=15V,Tj=25°C, Unit : mA

IPM S1-series	N-side				P-side (1 phase)			
	DC		20kHz		DC		20kHz	
Type. Name	Typ	Max	Typ	Max	Typ	Max	Typ	Max
PM50CS1D060	6	12	20	26	2	4	7	9
PM75CS1D060	6	12	25	33	2	4	9	12
PM100CS1D060	6	12	32	42	2	4	10	13
PM150CS1D060	6	12	41	53	2	4	14	18
PM200CS1D060	6	12	52	63	2	4	17	22
PM25CS1D120	6	12	22	29	2	4	8	10
PM50CS1D120	6	12	36	47	2	4	13	17
PM75CS1D120	6	12	49	64	2	4	17	22
PM100CS1D120	6	12	65	85	2	4	21	29

The circuit current of control power supply of IPM increases with the carrier frequency.
The carrier frequency dependence of the circuit current of the IPM control power supply can be approximated as a straight line like the following figure.





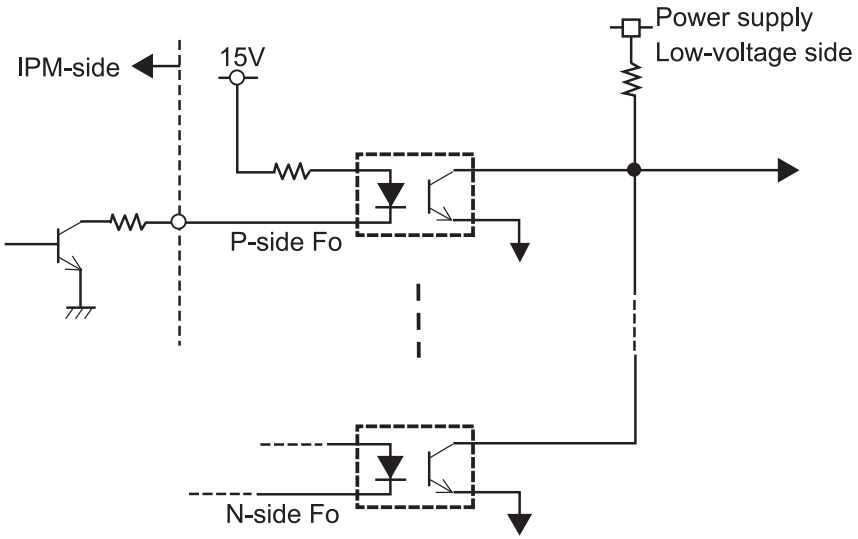
The gate of IGBT used in IPM has an input-capacitance (Cies =C_{GE}+C_{CG}).
The current to be charge and discharged by flowing through the gate at the timing of gate on and off.
There is IPM that this current becomes 1~2 A.

When IPM is turn-off, the dv/dt current from the collector of IGBT flows into the side of the control power supply. Design a control power supply in the low impedance so that this dv/dt current can be absorbed. Otherwise, The control IC of IPM might make malfunction and On signal is activated by this current resulting arm short circuit.

The control power supply circuit needs a capacity that it can supply and absorb these current.
Usually, such problems (maximum current, impedance) can be avoided by power supply circuit and also bypass, smoothing condenser. But, the effect of the condenser is influenced by the inductance of the wiring pattern. Determine the condenser capacity after verifying the substrate and the equipment.

11-11. Fo Circuit

In order to keep the interface circuits simple the IPM uses a single on/off output to alert the system controller of all fault conditions. The system controller can easily determine whether the fault signal was caused by an over temperature or over current/short circuit by examining its duration. Short circuit and over current condition fault signals will be t_{FO} (typical 1.8ms) in duration.



Unused fault outputs of P-side

Unused fault outputs must be properly terminated by connecting them to the “+15V” on the local control power supply. Failure to properly terminate unused fault outputs may result in unexpected tripping of the modules internal protection.

When not using Fo by the P-side, protection coordination cannot be carried out to the earth fault, which goes only via the P-side. The protected operation of IPM assumes the abnormality of a non-repetition. IPM may be destroyed, if an abnormal condition is repeated and stress is added to IPM. Please make protection coordination by the system side to the abnormality caused repeatedly.

12. Power Loss and Junction Temperature

Junction temperature can be used as an indication of IGBT module situation. This section will discuss how to calculate junction temperature and give an example based on waveform shown in Fig.12.1. Here, only power loss of IGBT part is given. The power loss of Diode can be obtained by using the same method as IGBT part. Moreover, junction temperature must never be outside of the maximum allowable value. It also has impact on the power cycle life.

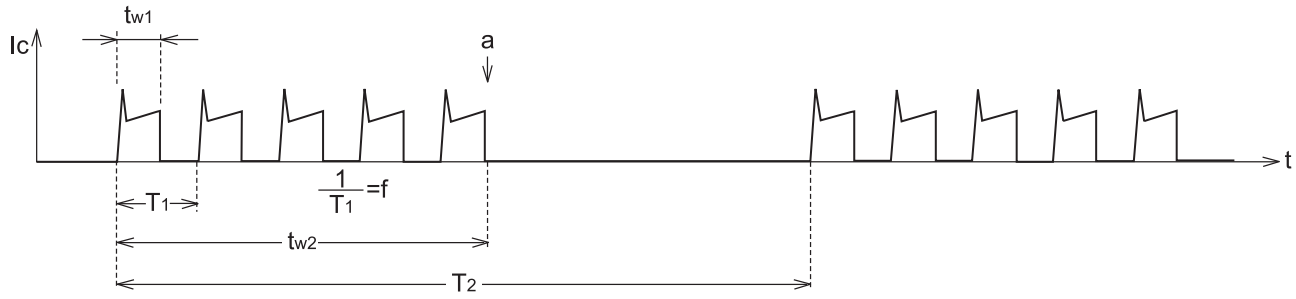


Fig.12.1

a. Power Loss

In order to estimate junction temperature for thermal design, it is necessary to compute total power loss. The first step is the calculation of power loss per pulse.

Two most important sources of power dissipation that must be considered are conduction losses and switching losses. (Fig.12.2)

(1) Conduction Losses

The total power dissipation during conduction is computed by multiplying the on-state saturation voltage by the on-state current.

$$E_{(sat)} = \frac{I_{C1} \times V_{CE(sat)1} + I_{C2} \times V_{CE(sat)2}}{2} \times t_{w1} \quad (J)$$

Note)The above equation is a simplification of the below one

$$E_{(sat)} = \int_0^{tw'} I_C(t) \bullet V_{CE}(t)dt$$

VCE(sat) VS. Ic characteristics at Tj=125°C is used in power loss calculation.

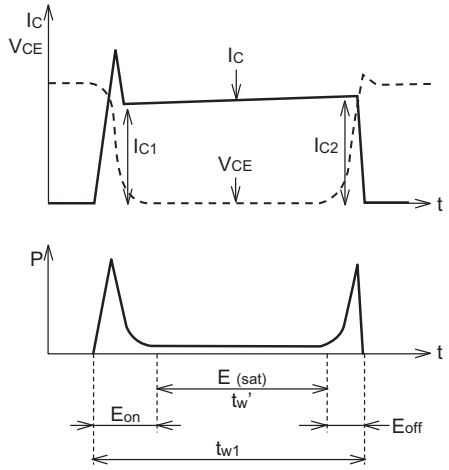


Fig.12.2

(2) Switching Losses

The most accurate method of determining switching losses is to plot the Ic and VCE waveforms during the switching transition. Multiply the waveforms point by point to get an instantaneous power waveform. The area under the power waveform is the switching energy expressed in watt-seconds/pulse or J/pulse.

$$E_{on} = \int_{ta}^{tb} I_C(t) \bullet V_{CE}(t)dt = \frac{1}{n}\sum_{n-1}^{n} P_n \times (t_b - t_a)$$

n: number of partitions

(divide interval between ta and tb equally into n parts, compute average power loss for each interval.)

Calculation of Eoff has the same method.

The total power loss of one pulse is the sum of (1) and (2).

$E_1 = E_{(sat)} + E_{on} + E_{off}$

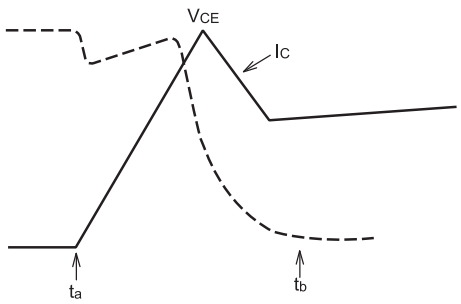


Fig.12.3

(3) Average Power Loss

The average power loss per pulse is

$$P_1 = \frac{E_1}{t_{w1}} \quad (W)$$

Fig.12.4 is approximation of Fig.12.1 by using rectangle wave.

Fig.12.4

Average power loss during period of tw2 is (See Fig.12.5)

$$P_{av} = \frac{E_1}{t_{w2}} \times N \quad (W)$$

N : pulse numbers in tw2 period

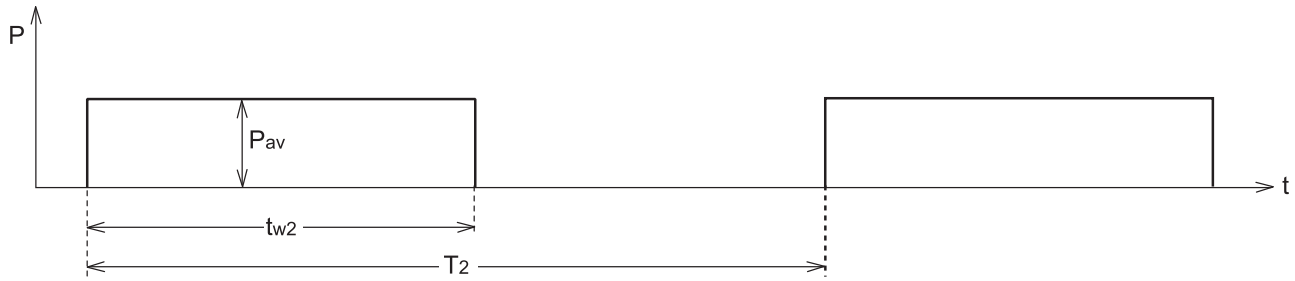


Fig.12.5

Total average power loss is (See Fig.12.6)

$$P_{AV} = P_{av} \times \frac{t_{w2}}{T_2} \quad (W)$$

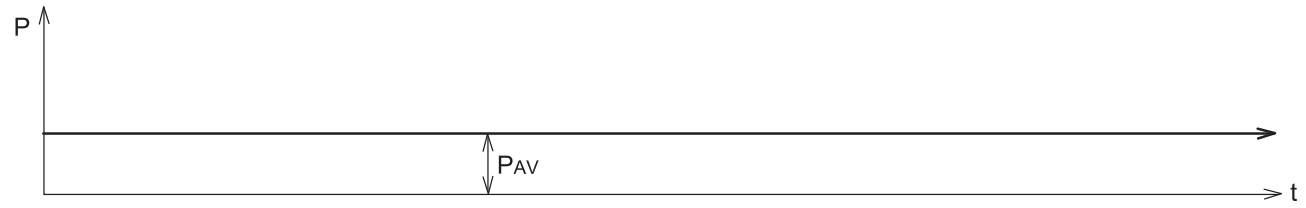


Fig.12.6

b. Junction Temperature Calculation

Junction temperature can be calculated by using P1, Pav, and PAV that has been obtained so far. Three cases should be considered according to pulse width.

(1) tw1 is short (tw1<<1ms)
(2) Both of tw1 and tw2 are long(1ms<tw1<tw2<1s)
(3) tw2 is longer than 1s.(tw2>1s)

(1) tw1<<1ms

In case of short on interval or low duty as in Fig.12.5, Junction temperatures rise to the highest value at the turn-off moment of tw2 while the case temperature is stationary. (See Fig.12.7)

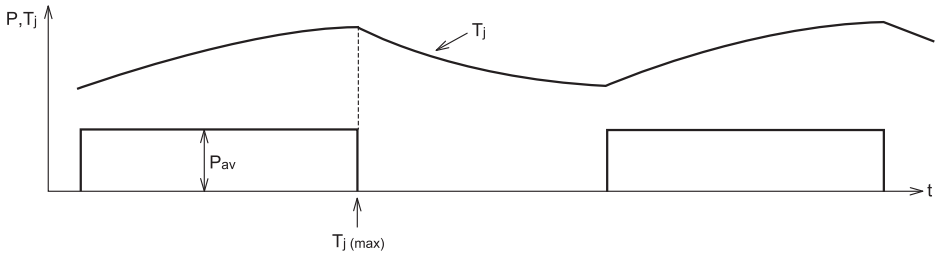


Fig.12.7

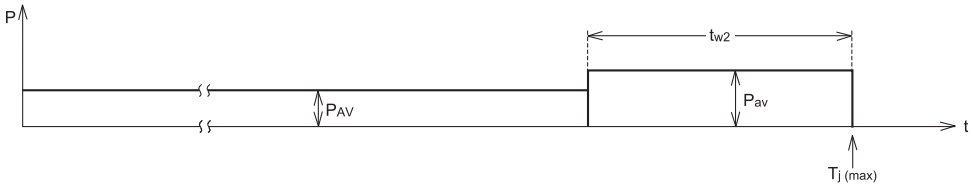


Fig.12.8

Temperature difference between junction and case can be calculated by using the following formula.

$\triangle T(j\text{-}c) = R_{th(j\text{-}c)} \times P_{AV} - Z_{th(j\text{-}c)(tw2)} \times P_{AV} + Z_{th(j\text{-}c)(tw2)} \times Pav = R_{th(j\text{-}c)} \times P_{AV} + (Pav - P_{AV}) \times Z_{th(j\text{-}c)(tw2)}$

$R_{th(j\text{-}c)}$ ……thermal resistance between junction and case

$Z_{th(j\text{-}c)(tw2)}$ ……thermal impedance between junction and case at tw2 moment

$\therefore Tj = Tc + \triangle T(j\text{-}c)$ (Tc is measured by thermo-couple.)

Tj(max)=150°C, therefore the allowable case temperature Tc(max) is, Tc(max)=150-△T(j-c).

(2) 1ms<tw1<tw2<1s

In this case, ripple should be considered in calculation of average power loss P1.

Using approximation similar to (1) Fig.12.9 is obtained for calculation.

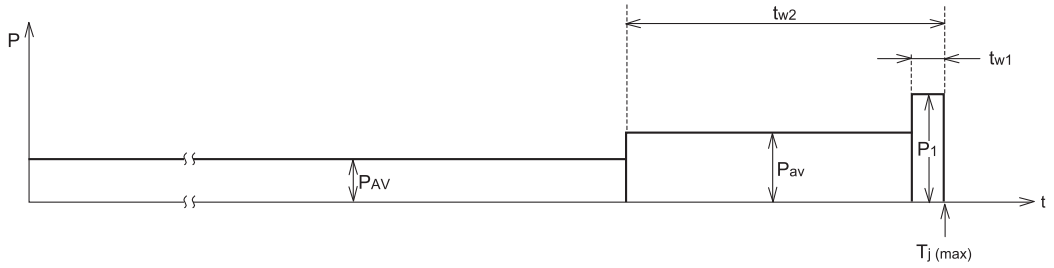


Fig.12.9

$\triangle T(j\text{-}c) = R_{th(j\text{-}c)} \times P_{AV} - Z_{th(tw2)} \times PAV + Z_{th(j\text{-}c)(tw2)} \times Pav - Z_{th(j\text{-}c)(tw1)} \times Pav + Z_{th(j\text{-}c)(tw1)} \times P1$

$= R_{th(j\text{-}c)} \times P_{AV} + (Pav - P_{AV}) \times Z_{th(j\text{-}c)(tW2)} + (Pl - Pav) \times Z_{th(j\text{-}c)(tw1)}$

$R_{th(j\text{-}c)}$ ……thermal resistance between junction and case

$Z_{th(j\text{-}c)(tw2)}$ ……thermal impedance between junction and case at tw2 moment

$Z_{th(j\text{-}c)(tw1)}$ ……thermal impedance between junction and case at tw1 moment

$\therefore Tj = Tc + \triangle T(j\text{-}c)$ (Tc is measured by thermo-couple.)

$Tc(max) = 150 - \triangle T(j\text{-}c)$

(3) tw2>1s

In a similar way to (2), temperature change of heat-sink should be taken into consideration as well. It is necessary to know the transient heat impedance of the heat-sink. (Fig.12.9)

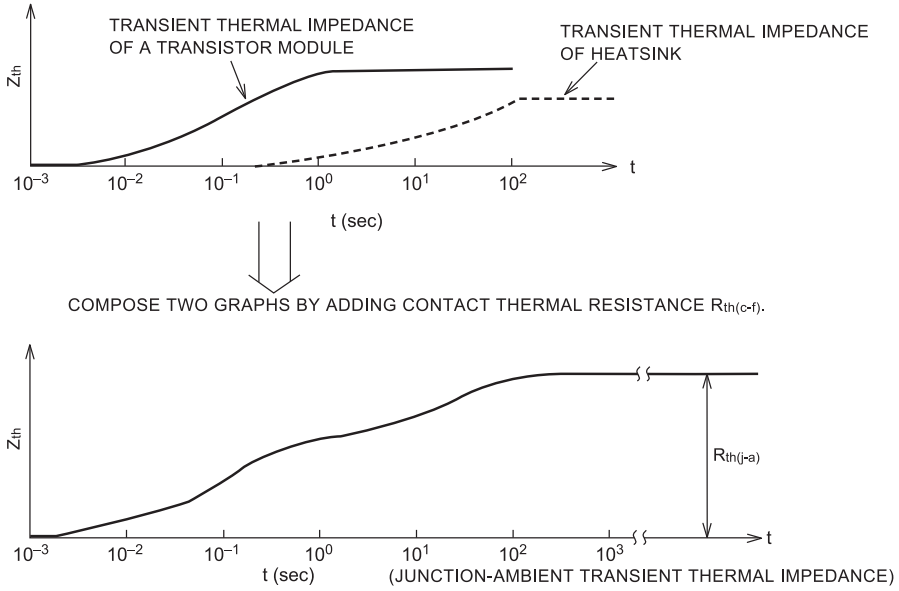


Fig.12.9

Similarly, the temperature difference between junction and ambient can be calculated by using the following formula.

$$\triangle T(j\text{-}a) = R_{th(j\text{-}a)} \times P_{AV} - Z_{th(j\text{-}a)(tw2)} \times P_{AV} + Z_{th(j\text{-}a)(tw2)} \times Pav - Z_{th(j\text{-}a)(tw1)} \times Pav + Z_{th(j\text{-}a)(tw1)} \times P1$$
$$= R_{th(j\text{-}a)} \times P_{AV} + (P_{av} - P_{AV}) \times Z_{th(j\text{-}c)(tw2)} + (P1 - Pav) \times Z_{th(j\text{-}c)(tw1)}$$
$$\therefore Tj = Ta + \triangle T(j\text{-}a) \quad \text{(Ta is measured by a thermometer.)}$$

c. Heat-sink Selection

Fig.12.10 shows the thermal equivalent circuit when two or more modules are mounted on one heat sink.

According to this equivalent circuit, the temperature of the heat sink is

$Tf = Ta + (P_{T(AV)} + P_{D(AV)}) \times NxR_{th(f\text{-}a)}$

Ta : Ambient temperature
$P_{T(AV)}$:Average power loss of IGBT
$P_{D(AV)}$:Average power loss of FWDi
N: Arm number
$R_{th(f\text{-}a)}$:The heat-sink to ambient thermal resistance

The case temperature Tc is,

$Tc = Tf + (P_{T(AV)} + P_{D(AV)}) \times R_{th(c\text{-}f)}$

Rth(c-f) : The case to heat-sink thermal resistance

Tc(max) can be calculated by using the below formula.

$\therefore T_{c(max)} = Ta + (P_{T(AV)} + P_{D(AV)}) \times NxR_{th(f\text{-}a)} + (P_{T(AV)} + P_{D(AV)}) \times R_{th(c\text{-}f)}$

Therefore, the heat-sink to ambient thermal resistance can be computed as

$$R_{th(f-a)} = \frac{T_{C(max)} - Ta - (P_{T(AV)} + P_{D(AV)}) \times R_{th(c-f)}}{(P_{T(AV)} + P_{D(AV)}) \times N}$$

Moreover, power loss of FWDi should be considered as well. In thermal design, the allowable case temperature Tc(max) is up to the smaller one of IGBT power loss and FWDi part.

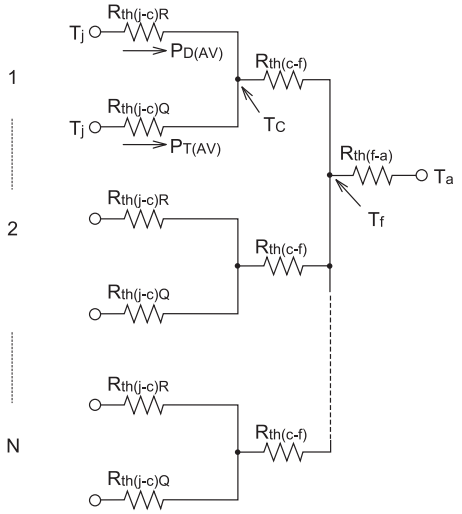


Fig.12.10 Thermal Calculation Model

13. Average Power Loss Simplified Calculation

(1) VVVF Inverter

■Applicability Range

It is applicable to total power loss calculation for selection of IGBTs used in VVVF inverters.
It is not applicable in the thermal design of the device (limit design).

■Assumption Condition

① PWM modulation used to synthesize sinusoidal output currents in VVVF inverters
② PWM signal generated by comparing sinusoidal wave to triangular wave
③ Duty cycle of PWM among the rank of $\frac{1-D}{2} \sim \frac{1+D}{2}(\%/100)$ D : modulation rate
④ Output current of $I_{CP}\cdot\sin x$ without ripple
⑤ With inductive load rate of cos θ

■Calculation Equation

Duty cycle of PWM is constantly changing and its value equal to time x $\frac{1+D\times\sin x}{2}$ at the corresponding moment.
The output current corresponds to the output voltage change and this relationship is represented by power factor cos θ . Therefore, the duty cycle of PWM corresponding to output current at arbitrary phase x is

$$\text{Output current} = Icp\times\sin x$$

$$\text{PWM Duty} = \frac{1+D\times\sin(x+\theta)}{2}$$

$V_{CE(sat)}$ and V_{EC} at this moment are

$$Vce(sat) = Vce(sat)(@Icp\times\sin x)$$

$$Vec = Vec(@(-1)\times Iecp(=Icp)\times\sin x)$$

Static power loss of IGBT is

$$\frac{1}{2\pi}\int_0^{\pi}(Icp\times\sin x)\times Vce(sat)(@Icp\times\sin x)\times\frac{1+D\sin(x+\theta)}{2}\bullet dx$$

Similarly, static power loss of FWDi is

$$\frac{1}{2\pi}\int_{\pi}^{2\pi}((-1)\times Icp\times\sin x)\times(Vec(@(-1)\times Icp\times\sin x)\times\frac{1+D\sin(x+\theta)}{2}\bullet dx$$

On the other hand, dynamic power loss of IGBT is not dependent on the PWM duty and can be expressed as the following formula.

$$\frac{1}{2\pi}\int_0^{\pi}(Psw(on)(@Icp\times\sin x)+Psw(off)(@Icp\times\sin x))\times fc\bullet dx$$

As for dynamic power loss of free-wheeling diode, calculation is given by an example of ideal diode shown in Fig.13.1.

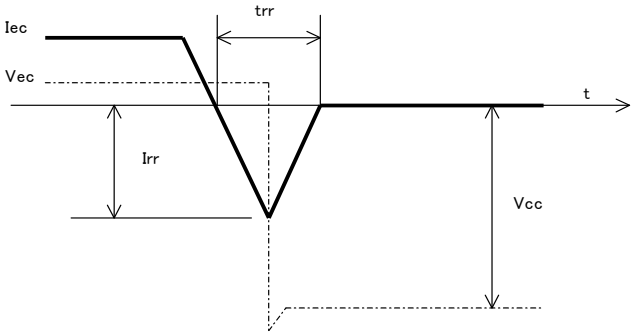


Fig.13.1. Dynamic Power Loss of FWDi

$$Psw = \frac{Irr \times Vcc \times trr}{4}$$

Because reverse recovery of free-wheeling diodes occurs in half cycle of the output current, the dynamic power loss of FWDi is

$$\frac{1}{2}\int_{\pi}^{2\pi} \frac{\mathrm{Irr}(@\mathrm{Icp}\times\sin x)\times \mathrm{Vcc}\times \mathrm{trr}(@\mathrm{Icp}\times\sin x)}{4}\times \mathrm{fc}\bullet dx$$
$$= \frac{1}{8}\int_{\pi}^{2\pi} \mathrm{Irr}(@\mathrm{Icp}\times\sin x)\times \mathrm{Vcc}\times \mathrm{trr}(@\mathrm{Icp}\times\sin x)\times \mathrm{fc}\bullet dx$$

■Inverter Loss Calculation Notes

・Divide one cycle of output current into many equal intervals, then calculate actual "PWM duty", "Output current", and "$V_{CE(sat)}$, V_{EC}, and Psw responding to the current" in each interval. The power loss during one cycle is the sum of each interval.

・The PWM duty depends on the method of generating the signal.

・The output current waveform and the relationship between output current and PWM duty cycle are dependent on signal generator, load and other factors. Therefore, calculation should always be done with actual waveforms.

・$V_{CE(sat)}$ uses the value of Tj=125°C.

・Psw uses the value under half bridge operating case at Tj=125°C.

■ Thermal Design Notes

① It is necessary to examine the worst switching condition.

② Consideration of temperature variation due to current cycle should be given in thermal design.
(Temperature variation rate is 30% to 35% for 60Hz case. When the output current of several Hz switches for a few seconds, it almost has equal temperature to a direct current with the same peak value continuously flowing.)

③ Temperature ripple caused by switching operation should be considered especially when switching frequency is much lower than 10kHz.

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